SERVICE MANUAL

(WITHOUT PRICE)

HAND-HELD COMPUTER

FP-200 (PX-1)

AUGUST 1983

CASIO®

CONTENTS

1. INTRODUCTION

This service manual is intended for service technicians who will work with the Casio FP-200 hand-held computer. It will allow the technician to provide prompt and accurate after-sales repair/maintenance.
Though the contents of this manual are as simple and clear as possible, the manual is still aimed at electronically oriented technicians who already have some experience in computer hardware and have an understanding of transistor theory.

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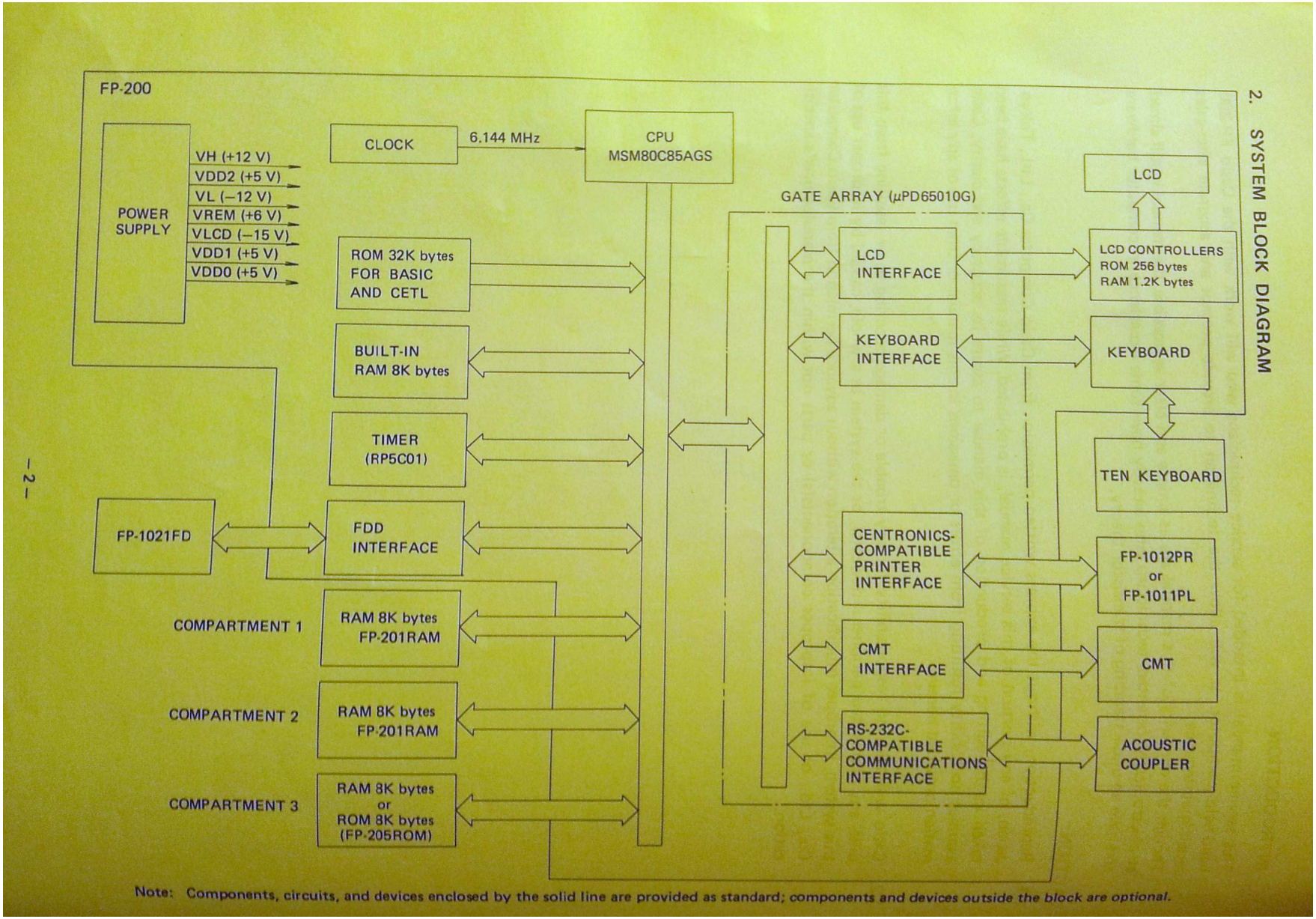


Note: Components, circuits, and devices enclosed by the solid line are provided as standard; components and devices outside the block are optional.

3. SPECIFICATIONS

CPU

- MSM80C85AGS 8-bit microprocessor.
- 6.144 MHz clock frequency.
- Compatible with INTEL8085.
- One wait period (one clock cycle added) for RAM and ROM access.
- Two wait periods (two clock cycles added) for I/O device access.

RAM

- 8K bytes built-in (standard) and can be expanded to 32K bytes.

ROM

- 32K bytes built-in (standard) for BASIC and CETL interpreters.
- Expandable to 40K bytes.

DISPLAY

- Liquid Crystal Display (LCD)
- 1/64 duty cycle
- Adjustable contrast
- Capacity of display
  - In text mode: 20 characters x 8 lines (160 characters)
  - In graphics mode: 64 (H) x 160 (W) dots (10,240 dots)
  - Number of dots per character: 8 x 8 (16 dots)

I/O INTERFACE CONTROLLER

- μPD65010G (GATE ARRAY)
- Kansas City standard for CMT
- Centronics (parallel) standard for printer and mini-plotter.
- RS-232C (serial) standard for I/O port.

INTERFACE

- CMT: Baud rate 300
  Remote control
  Input/output specifications

MIC	Output impedance	5 KΩ
	Output voltage	3 mVp-p
EAR	Input impedance	10 KΩ
	Input voltage	3 – 10 Vp-p
Remote		DC 24 V, 1 A or less

- PRINTER: 8-bit parallel output
  Data transfer via handshaking
- Communication: Compatible with RS-232C standard
  Serial I/O
  Baud rate 300
  Half-duplex transmission

POWER SOURCE

- AD4180 adaptor (+6 V output) for AC-powered operation and use of mini-floppy disk drive FP-1021FD, graphics printer FP-1012PR, mini-plotter FP-1011PL, and RS-232C interface.
- SUM-3 (4 pcs) for DC-powered operation
- SUM-3 (2 pcs) for memory backup
- Battery life expectancy
  Operating battery: 6 hours for SUM-3 or 11 hours for AM-3 (4 batteries)
  Memory backup battery: 6 months for SUM-3 (2 batteries)

OPERATING ENVIRONMENT

- Temperature 0 – 40°C (32 – 104°F)
- Humidity 20 – 85%

DIMENSIONS

- 310 (W) x 220 (D) x 55.5 (H) mm

NET WEIGHT

- 1.54 Kg (3.4 lb)

4. ADDRESS MAPS

4-1. MEMORY MAP

The CPU in the FP-200 hand-held computer has 16 address lines and can address 65,536 bytes (64K) by changing its high-low signal status timesharingly.
As built-in standard memory, the first 32K from 0000H to 7FFFH is allocated to ROM, which contains fixed data and the BASIC and CETL interpreters; the next 8K (8000H to 9FFFH) is RAM used for the system work area, available to BASIC and CETL programs.
Besides this 40K of memory, up to 24K of RAM or up to 16K of RAM and 8K of ROM (a total of 24K of memory) can be added easily by installing optional RAM pack FP-201RAM and ROM pack FP-205ROM in the FP-200's compartments.
The entire memory structure is shown below. Adresses are in hexadecimal.

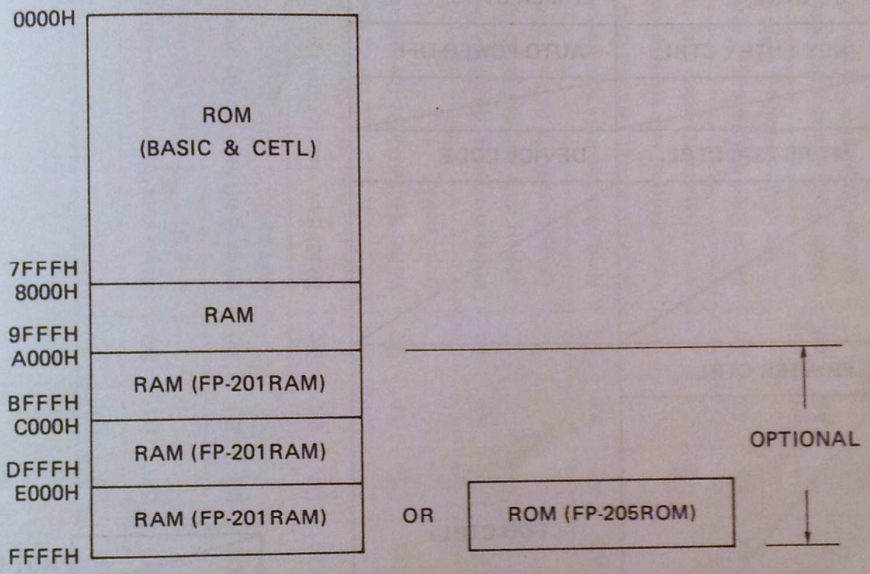


Fig. 4-1 MEMORY MAP

4-2. I/O ADDRESS MAP

To control and access I/O devices in this unit, I/O addresses are allocated as shown below. This I/O address map is two pages by output from the SOD (serial output data) terminal of the CPU by changing its output status bit 1 or 0. This causes the address map to be switched to the other side (left or right) to control access the I/O device functions.
When an I/O device is addressed, the 8 low-address lines (AD0 to AD7) are used, enabling the designation of any of up to 256 addresses for each page.

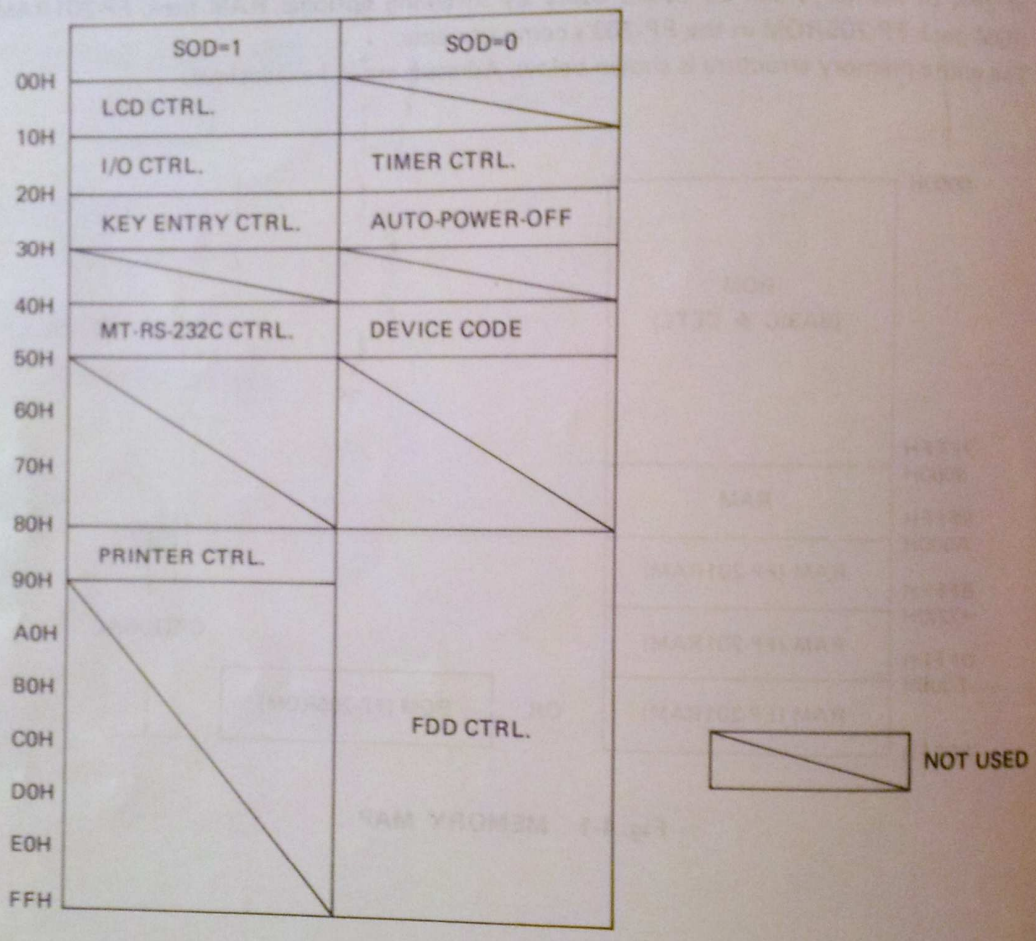


Fig. 4-2 I/O ADDRESS MAP

4-3. DETAILED I/O ADDRESS MAP

On this page, the I/O address explained briefly on the previous page will be explained in detail. It is strongly recommended that the reader fully understand the I/O address map on the last page before going on to this page. Even then, he will find the previous page useful if used as a reference when reading this page.

SOD	ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
1	01	R	D7	D6	D5	D4	D3	D2	D1	D0	Reads data for the operation code in the LCD controller's RAM and transfers it to the LCD driver (left half).
1	01	W	D7	D6	D5	D4	D3	D2	D1	D0	Writes 8-bit data for the operation code in the LCD controller's RAM (left half).
1	02	R	D7	D6	D5	D4	D3	D2	D1	D0	Reads 8-bit data for the operation code in the LCD controller's RAM and transfers it to the LCD driver (right half).
1	02	W	D7	D6	D5	D4	D3	D2	D1	D0	Writes 8-bit data for the operation code in the LCD controller's RAM (right half).
1	08	W	S3	S2	S1	S0	–	–	A9	A8	Writes 6-bit data (S0-S3 for the status code and high 2 bits of the 6-bit address data that designates the address allocated in 00-3F for Y) in the LCD controller's RAM (left or right half).
1	09	R	A7	A6	A5	A4	A3	A2	A1	A0	Reads 8-bit address data (low 4 bits of address data (A0-A3)) for the X address and high 4 bits of address data (A4-A7) which reforms 6-bit address data with other 2 bits of address data (A8-A9) for the Y address) in the LCD controller's RAM and transfers it to the LCD driver (left or right half).
1	09	W	A7	A6	A5	A4	A3	A2	A1	A0	Writes 8-bit address data (A0-A3) for X and (A4-A7) for part of the Y address in the LCD controller's RAM (left or right half).
1	08	R	S3	S2	S1	S0	–	–	A9	A8	Reads 6 bits of status data and Y address data (written by the operation at address 08) and "W" in the LCD controller's RAM and transfers it to the LCD driver (left or right half).
1	10	R	–	–	–	–	–	E	–	R	If D0 is 0 "READY" in a serial I/O device is set and if D2 is 1 "PAPER EMPTY" in printer is set.

SOD	ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
1	10	W	–	–	–	–	–	–	M	–	D1 indicates whether data is output to CMT or RS-232C (0 for CMT, and 1 for RS-232C port).
1	11	W	–	–	–	–	–	0	1	0	By writing 0 at bits D0 and D2 and 1 at bit D1 into gate array μPD65010G, ports P0 and P2 of the gate array are designated as input ports and P1 of the same is designated as an output port.

			MODE 00				MODE 01					
			FUNCTION	D3	D2	D1	D0	FUNCTION	D3	D2	D1	D0
0	10	R/W	SECOND CTR.	D3	D2	D1	D0	–	X	X	X	X
0	11	R/W	TEN-SECOND CTR.	X	D2	D1	D0	–	X	X	X	X
0	12	R/W	MINUTE CTR.	D3	D2	D1	D0	ALARM MINUTE REGISTER	NOT USED			
0	13	R/W	TEN-MINUTE CTR.	X	D2	D1	D0	ALARM TEN-MINUTE REGIST.	NOT USED			
0	14	R/W	HOUR CTR.	D3	D2	D1	D0	ALARM HOUR REGISTER	NOT USED			
0	15	R/W	TEN-HOUR CTR.	X	X	D1	D0	ALARM TEN-HOUR REGISTER	NOT USED			
0	16	–	WEEK CTR.	NOT USED				ALARM WEEK REGISTER	NOT USED			
0	17	R/W	DAY CTR.	D3	D2	D1	D0	ALARM DAY REGISTER	NOT USED			
0	18	R/W	TEN-DAY CTR.	X	X	D1	D0	ALARM TEN-DAY REGISTER	NOT USED			
0	19	R/W	MONTH CTR.	D3	D2	D1	D0	–	NOT USED			
0	1A	R/W	TEN-MONTH CTR.	X	X	X	D0	$\overline{12H}$/24H SELECTOR	NOT USED			
0	1B	R/W	YEAR CTR.	D3	D2	D1	D0	LEAP-YEAR REGISTER	NOT USED			
0	1C	R/W	TEN-YEAR CTR.	D3	D2	D1	D0	–	NOT USED			
0	1D	R/W	MODE REGISTER	TE	AE	M1	M0	MODE REGISTER	NOT USED			
0	1E	W	TEST REGISTER	T3	T2	T1	T0	TEST REGISTER	NOT USED			
0	1F	W	RESET CONTROL	1H	16H	TR	AR	RESET CONTROL	NOT USED			

X: DO NOT CARE AT WRITE AND 0 AT READ.

T3: TEST MODE 3
T2: TEST MODE 2
T1: TEST MODE 1
T0: TEST MODE 0

TE: TIMER ENABLE
AE: ALARM ENABLE

1H: 1 Hz ON
16H: 16 Hz ON
TR: TIMER RESET
AR: ALARM RESET
M1: MODE 01
M0: MODE 00

BITS D4-D7 ARE NOT USED.

MODE REGISTER

D3	D2	D1	D0	
TE	AL	M1	M0	
		0	0	→ SELECT MODE 00 FOR PROGRAMMING OF TIME AND READ OUT.
		0	1	→ SELECT MODE 01 FOR PROGRAMMING OF ALARM, $\overline{12H}$/24H, LEAP YEAR, AND READ OUT.
		1	0	→ SELECT WRITE/READ IN RAM OF BLOCK 10.
		1	1	→ SELECT WRITE/READ IN RAM OF BLOCK 11.
	→			IF 1 ENABLES ALARM OUTPUT, 0 DISABLES ALARM OUTPUT. 16 Hz AND 1 Hz SIGNALS ARE NOT AFFECTED.
→				TIMER STARTS COUNTING WHEN THE BIT IS 1 AND COUNTERS AFTER SECOND COUNTER STOP COUNTING WHEN THE BIT IS 0.

1	20	R	D7	D6	D5	D4	D3	D2	D1	D0	Reads data of keys from the buffer register.
1	21	W	–	–	–	–	D3	D2	D1	D0	Writes 4-bit data (00-0A) using low bits D0-D3 in the key common register in the gate array. High bits (D4-D7) are not used.
0	20	R	UNDEFINED								This I/O address is used when auto-power-off occurs.
1	40	R	–	–	–	–	D3	–	–	–	Data from CMT or RS-232C port is input to bit D3 of the CPU accumulator.
1	40	W	–	–	–	–	–	–	–	D0	Data at bit D0 of the accumulator is transfered to the gate array to be transfered to CMT or RS-232C port.
1	41	R	–	–	E	R	–	–	–	–	If D4 is 1, the serial data control circuit in the gate array is ready. If D4 is 0, the circuit is not ready. If D5 is 1, an error has occurred in the control circuit. These statuses are output from the gate array each time a byte of data is transferred.
1	41	W	D7	D6	D5	D4	D3	D2	D1	D0	Arbitrary data in bits D0-D7 are output to the gate array as an acknowledge signal for synchronization with the start bit when data from a serial I/O device is input to the CPU.

SOD	ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
1	43	W	—	—	—	0	0	M2	M1	M0	Bits D0-D2 are output from the CPU to the gate array to designate the status of port P1 and RMT in the gate array.
0	40	R	0	0	0	0	0	1	0	1	Read the device code of "05" from the mini-floppy disk drive unit (FP-1021FD) at power-on.
1	80	W	D7	D6	D5	D4	D3	D2	D1	D0	8-bit parallel data is output for the printer to the gate array once then output to the printer.
1	81	R	B	—	—	—	—	—	—	—	D7 is set to 1 to indicate that the line buffer of the Centronics standard printer is full, causing the CPU to temporarily stop transfer of 8-bit data to the printer.
0	80	R	RQM	DIO	NDM	CB	D3B	D2B	D1B	D0B	These indicate the read status of each bit of the status register in the FDC of the FP-1021FD. The CPU performs the appropriate disk operation according to this information. A bit set to 1 indicates there is a status, and a bit set to 0 indicates there is no status. D0B (D0): Drive 0 is executing a seek command or holding for an interrupt request for termination of the seek. D1B (D1): Same as for D0B except that it is drive 1 instead of drive 0.

M0 →

M STATUS AT ADDRESS 10	0		1	
M0 STATUS AT ADDRESS 43	0	1	0	1
REMOTE OF CMT	OFF	ON	OFF	OFF
RTS OF RS-232C PORT	OFF	OFF	OFF	ON

M1 →

0	OUTPUT MODE
1	INPUT MODE

M2 →

0	CMT MODE
1	RS-232C

SOD	ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
											D2B (D2): Same as for D0B except that it is drive 2 instead of drive 0. D3B (D3): Same as for D0B except that it is drive 3 instead of drive 0. CB (D4): FDC is now executing the execution phase of the phase command or the result phase of the ready write command, and cannot accept other commands as long as this bit is 1. NDM (D5): FDC is now transferring data in the non-DMA mode and is requesting service from the CPU. DIO (D6): Designates direction of data flow D6 is 0 if flow is from the CPU to the FDC. D6 is 1 if the flow is from the FDC to the CPU. Status of the data register is designated by RQM bit D7. RQM (D7): Indicates data to be transferred to the CPU from the FDC is being loaded or that there is no data in the data register and data from the CPU can be loaded in.
0	81	R	D7	D6	D5	D4	D3	D2	D1	D0	Reads 8-bit data from the data register of the FDC.
0	81	W	D7	D6	D5	D4	D3	D2	D1	D0	Writes 8-bit data in the data register of the FDC.
0	82	W	D7	D6	D5	D4	D3	D2	D1	D0	Writes 8 bits of random data in the input terminal TC of the FDC informing the FDC that the read or write operation from the CPU has ended.
0	84	W	D7	D6	D5	D4	D3	D2	D1	D0	Transfers (writes) 8 bits of random data to the FD control circuit of FP-1021FD, which is decoded to form the MOTOR ON signal.
0	86	W	D7	D6	D5	D4	D3	D2	D1	D0	Transfers 8 bits of random data to the FD control circuit, which is decoded to form the RESET signal.
0	86	R	INT	–	–	–	–	–	–	R	Reads status bits D0 and D7 from the status register in the FDC. If D0 is 1, the FDC is ready to receive data, and if D7 is 1, an interrupt from the FDC has been made to the CPU.

5. DISASSEMBLY/ASSEMBLY

5-1. DISASSEMBLY

REMOVING UPPER HOUSING

1) Turn the power switch off and disconnect all peripheral devices. Also remove RAM and ROM packs from their compartments.
2) Remove 4 screws at each corner of the lower housing.
3) Unhook the 4 hooks from the upper housing (2 at the front and 2 at the rear), then lift the upper housing straight up.
4) While holding the upper housing, unplug the 2 flexible green cables with your other hand.
5) Disconnect the 2 green ground wires from the power supply section.

REMOVING DISPLAY PCB (P1-E2)

1) Remove 4 screws from each corner of the display PCB (P1-E2).

   WARNING: Never try to remove the LCD or the three LSI chips (two of which are underneath the LCD). You must replace the entire PCB with a new one when one of these components fails.

REMOVING CONDUCTIVE RUBBER SHEET AND KEYTOPS

1) Remove 17 screws from the tops of the P1-E4 and P1-E3 PCBs, then remove the plastic spacer and the conductive rubber sheet.
2) To remove a keytop, unhook the two diagonal hooks while the upper housing is lifted-up so that the key top will drop down by itself when the two hooks are released as shown in Fig. 5-1.

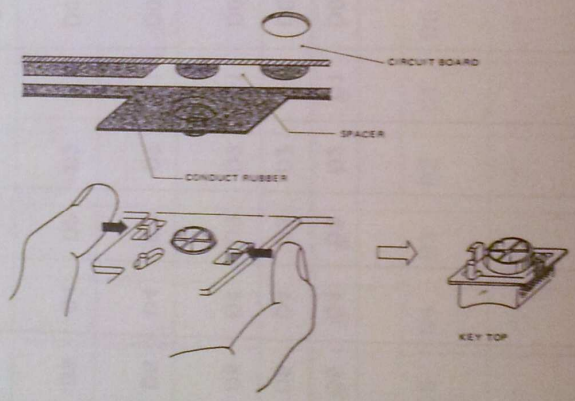


Fig. 5-1 REMOVING KEY TOP

REMOVING MAIN PCB (P1-1)

1) Remove the battery compartment for the operating battery, then remove 2 screws holding FDD connector on the chassis with a phillips screwdriver through the slot.
2) Remove 6 screws (4 on top of the main PCB and 2 on top of the power supply PCB (P1-1)). Disconnect the five-pin power connector and turn over the power supply PCB to the left as if you were opening a page in a book.
   Note the metal collars around the two shafts that sit on the power supply PCB. Take these collars away but not to loose.
3) Remove 3 screws holding the PCB (P1-B) that the printer connector, CMT connector, and RS-232C port connector are located on. Remove the PCB.

5-2. ASSEMBLY

Assembly is simple — just reverse all the steps in the disassembly procedure.

6. EXPLANATION OF CIRCUITS

6-1. CPU (MSM80C85A)

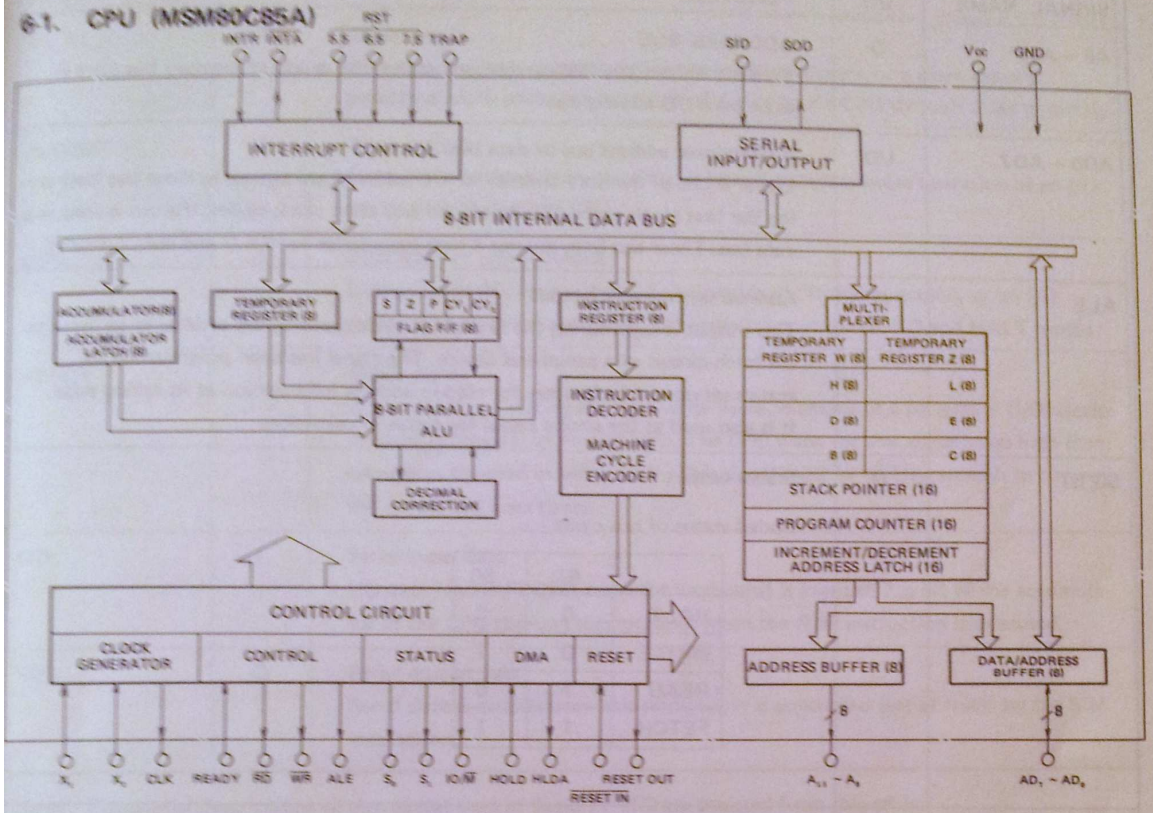


Fig. 6-1 CPU BLOCK DIAGRAM

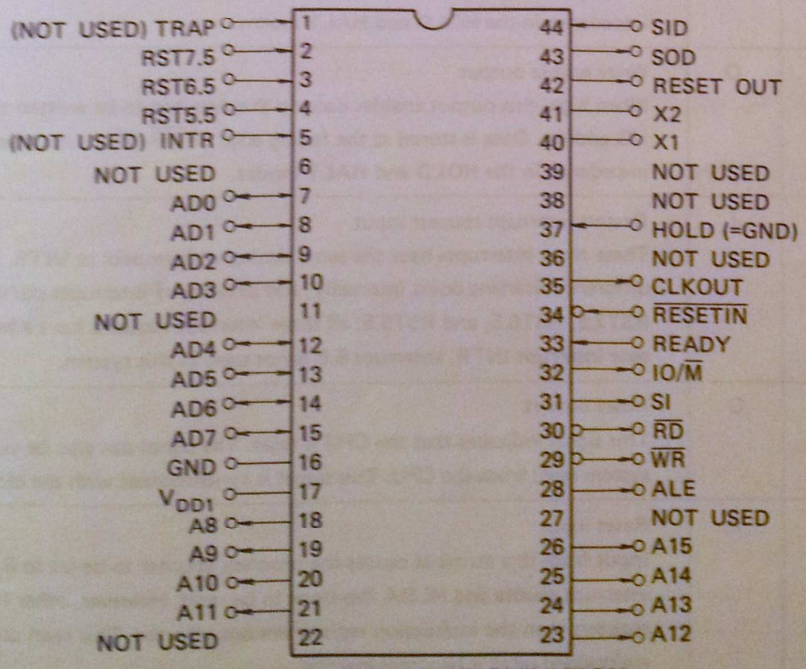


Fig. 6-2 PIN CONFIGURATION

SIGNAL NAME	I/O	FUNCTION
A8 – A15	O	ADDRESS BUS An 8-bit address bus that can be used as the high group of memory bus lines or as an 8-bit I/O address bus.
AD0 – AD7	I/O	Bidirectional address bus or data bus. Lower 8 bits of memory address (or I/O address) are output to these bus lines during the first clock cycle. During second and third clock cycles, the bus is used as a data bus. These bus lines assume a high impedance in HOLD and HALT modes.
ALE	O	Address latch enable output This output is high during the first clock cycle, causing the address to be input to the latch circuit of a peripheral device. The signal has been programmed to ensure set-up and hold times for read-in address information at its falling edge. It is also used as the strobe signal for status information.
S0, S1	O	Status output Coded status of bus cycle. HALT: S1 = 0, S0 = 0 WRITE: S1 = 0, S0 = 1 READ: S1 = 1, S0 = 0 FETCH: S1 = 1, S1 = 1
$\overline{RD}$	O	Read enable output When high, this output enables reading of selected memory or I/O address and indicates that the data bus is being used for data transfer. It assumes a high impedance in the HOLD and HALT modes.
$\overline{WR}$	O	Write enable output When high, this output enables data on the data bus to be written to a memory or I/O address. Data is stored at the falling edge of $\overline{WR}$. The output assumes a high impedance in the HOLD and HALT modes.
RST5.5 RST6.5 RST7.5	I	Restart interrupt request input These three interrupts have the same timing with respect to INTR. Each has different restarting point internally, and priority of interrupts starts from RST7.5, RST6.5, and RST5.5; all three interrupt requests have a higher priority over interrupt INTR. Interrupt 5.5 is not used in this system.
RESET OUT	O	Reset output This signal indicates that the CPU is reset. The signal can also be output as a system reset from the CPU. This signal is synchronized with the clock.
$\overline{RESET\ IN}$	I	Reset input Input from this terminal causes the program counter to be set to 0 and both the interrupt enable and HLDA flip-flops to be reset. However, other flags and registers than the instruction register are not affected. This reset condition is maintained until it becomes inactive.

SIGNAL NAME	I/O	FUNCTION
X1, X2	I/O	Clock input A crystal oscillator is connected to these two terminals, or a clock signal is generated and transferred by periphral device to the CPU through these terminals.
CLKOUT	O	Clock output Output of the clock from the CPU; it is used to synchronize operation of an I/O device with that of the CPU.
IO/$\overline{M}$	O	Data transfer cntrol output Output from this terminal designates read/write from/to memory or an I/O device. The terminal assumes a high impedance in the HOLD and HALT modes.
READY	I	Ready signal If this signal is 1 during the read/write cycle, memory or a peripheral (I/O) device is ready to transfer or receive data. The CPU waits for this signal to go high then completes the read or write cycle. This signal must be on long enough to ensure the set-up and hold times.
SID	I	Serial input data I/O data (in the FP-200, from the keyboard) is input to 7th bit of the accumulator in the CPU through this terminal when the RIM instruction is executed.
SOD	O	Serial output data Serial data is output from this terminal; it is controlled (set or reset) by the SIM instruction.

Note: Functional descriptions of signals not used in Casio FP-200 are omitted from this table.

OPERATIONAL TIMING CHART

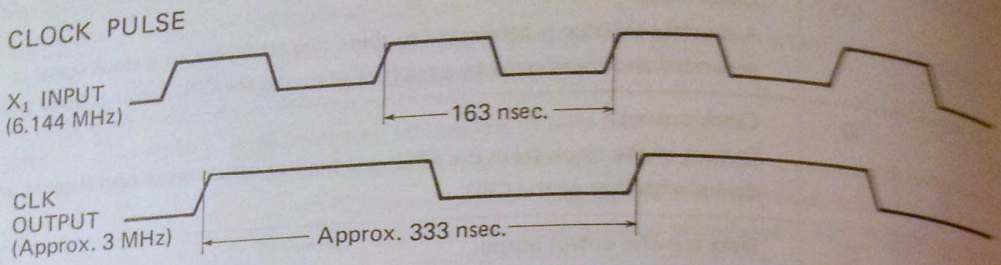


Fig. 6-3 CLOCK PULSE TIMING CHART

READ/WRITE CYCLE

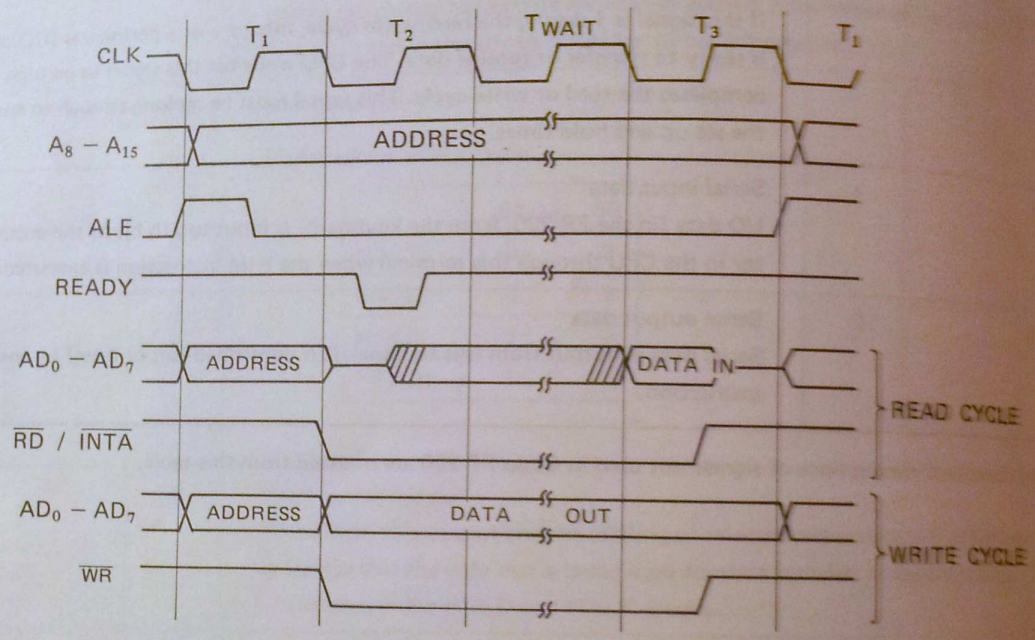


Fig. 6-4 READ/WRITE TIMING CHART INSTRUCTION FETCH CYCLE

INSTRUCTION FETCH CYCLE

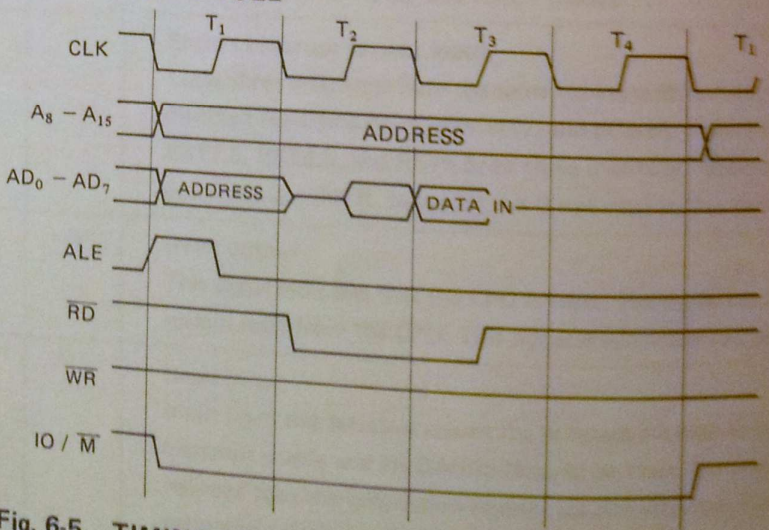


Fig. 6-5 TIMING CHART FOR INSTRUCTION FETCH CYCLE

6-2. GATE ARRAY (μPD65010G-030)

After the CPU, the next most important device in the FP-200 is the CMOS gate array. The gate array interfaces between the CPU and I/O devices such as a Centronics-compatible printer, RS-232C port, etc.; the gate array simplifies the entire system. The gate array programmed for FP-200 can access the LCD display, RS-232C port, printer, mini-plotter, CMT, and the keyboard.

PIN CONFIGURATION

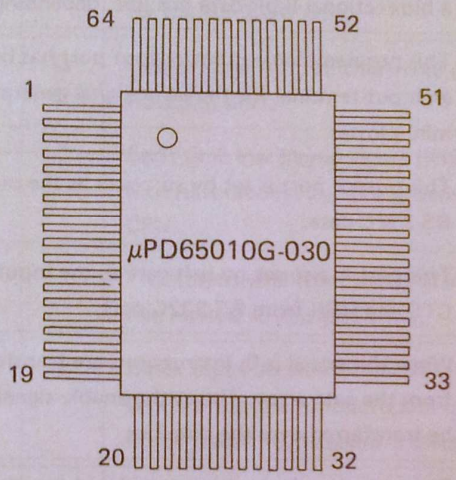


Fig. 6-6 PIN CONFIGURATION FOR GATE ARRAY μPD65010G-030

BLOCK DIAGRAM OF GATE ARRAY

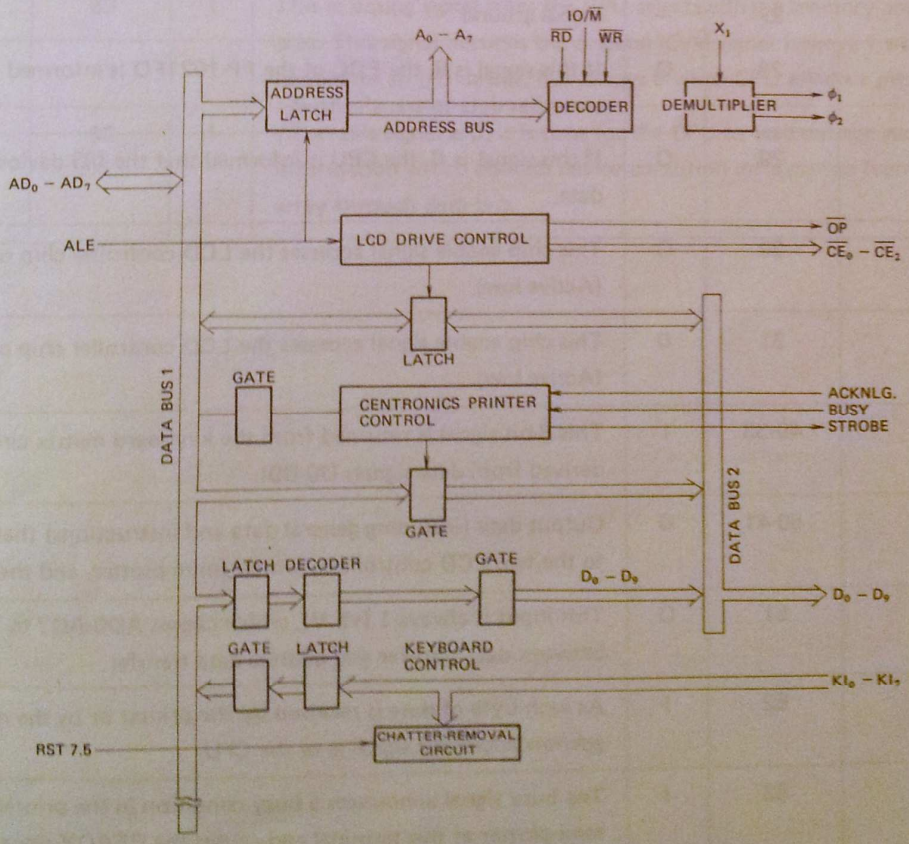


Fig. 6-7 BLOCK DIAGRAM OF GATE ARRAY

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
$\overline{WR}$	2	I	The write enable signal is generated by the CPU and causes the CPU to write data to the gate array when it is 0. (Active low)
A0 – A7	11-4	O	The low group of address bits are derived from address outputs AD0-AD7 which are latched by the ALE signal.
AD0 – AD7	19-12	I/O	This 8-bit bus line can be used as either a low-address bus lines (A0-A7) or a bidirectional 8-bit data bus line, depending on the clock state.
P2	20	I	This programmable input/output port has been programmed for use as an input terminal for the error signal generated by the printer or the mini-plotter.
P1	21	O	This output port is set by software as the output port for CMT data or RS-232C data.
P0	22	I	This port is also set by software as the input port for the decoded signal of CTS and DSR from RS-232C port.
$\overline{OP}$	23	O	When this signal is 0, instructions are transferred to the LCD controller from the gate array. This is the enable signal that allows instructions to be transferred over the data bus.
$\phi 1, \phi 2$	25, 24	O	These clock pulses are generated and transferred by the gate array to synchronize the LCD controller's operation.
VDD	26, 58	I	+5 V DC
GND	27	–	Signal ground
$\overline{CE4}$	28	O	If this signal is 0, the FDC of the FP-1021FD is informed that the gate array has data to transfer to it.
$\overline{CE3}$	29	O	If this signal is 0, the CPU is informed that the I/O device is ready for data.
$\overline{CE2}$	30	O	This chip enable signal accesses the LCD controller chip of the right half. (Active low)
$\overline{CE1}$	31	0	This chip enable signal accesses the LCD controller chip of the left half. (Active low)
KI0 – KI7	40-33	I	This 8-bit signal is returned from the keyboard matrix circuit (originally derived from data signals D0-D9).
D0 – D9	50-41	O	Output data (including general data and instructions) that is transferred to the two LCD controllers, printer, mini-plotter, and the keyboard.
CPUS	51	O	This input is always 1 (+5 V), which causes AD0-AD7 to be timeshared between data transfer and address data transfer.
ACKNLG	52	I	As each byte of data is received by the printer or by the mini-plotter, any acknowledgement signal is to the CPU.
BUSY	53	I	The busy signal announces a busy condition in the printer or in the mini-plotter at this terminal and causes the READY signal to reset (not active).

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
STROBE	54	O	This strobe signal is used to synchronize writing data to the printer buffer from the CPU.
RMT	55	O	If this signal is 1, the AND gate for the remote control circuit of CMT and the NAND gate circuit of RST for RS-232C port are enabled.
EAR	56	I	This input terminal is set for serial data for incoming port CMT and for the RS-232C port.
MIC	57	O	Output data from this terminal is serial data and is transferred to CMT or RS-232C port.
RST7.5	59	O	Each time low key-in signal (KI0-KI7) is input to the gate array, an interrupt request signal is generated and input to terminal RST7.5 of the CPU.
RST	60	I	This reset signal from the CPU initializes the registers, the counter, and the flag register in the gate array.
X1	61	I	Clock input derived from the CPU. This in the gate array signal is used to synchronize the functions and I/O derives controlled by the gate array. Clock frequency is about 3 MHz.
READY	62	O	This ready signal differs from the ready signal previously explained. This ready signal declares that the serial data control circuit of the gate array is ready to operate.
IO/$\overline{M}$	63	I	This selecting signal from the CPU selects either a memory area or I/O area. This signal decodes the original IO/$\overline{M}$ signal (always 1 when the CPU designates an I/O device, but always 0 when CPU selects a memory area).
$\overline{RD}$	64	I	When this signal is 0, it is time for the CPU to read data or status information which contain device condition information from the gate array through data bus.

6-3. TIMER (RP5C01)

A programmable timer used in this system, the RP5C01, can count time (hours, minutes and seconds), keep track of the date/month/year (including leap year), has two time indication modes (12-hour with AM and PM or 24-hour), etc.
It has also non-volatile (26 x 4 bits) RAM memory protected by an external back-up battery.

PIN CONFIGURATION

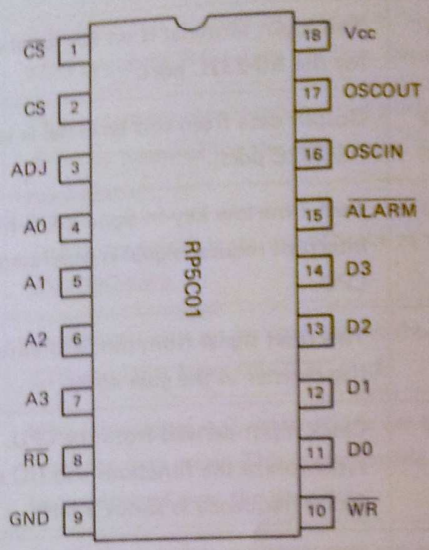


Fig. 6-8 PIN CONFIGURATION OF TIMER

BLOCK DIAGRAM OF TIMER

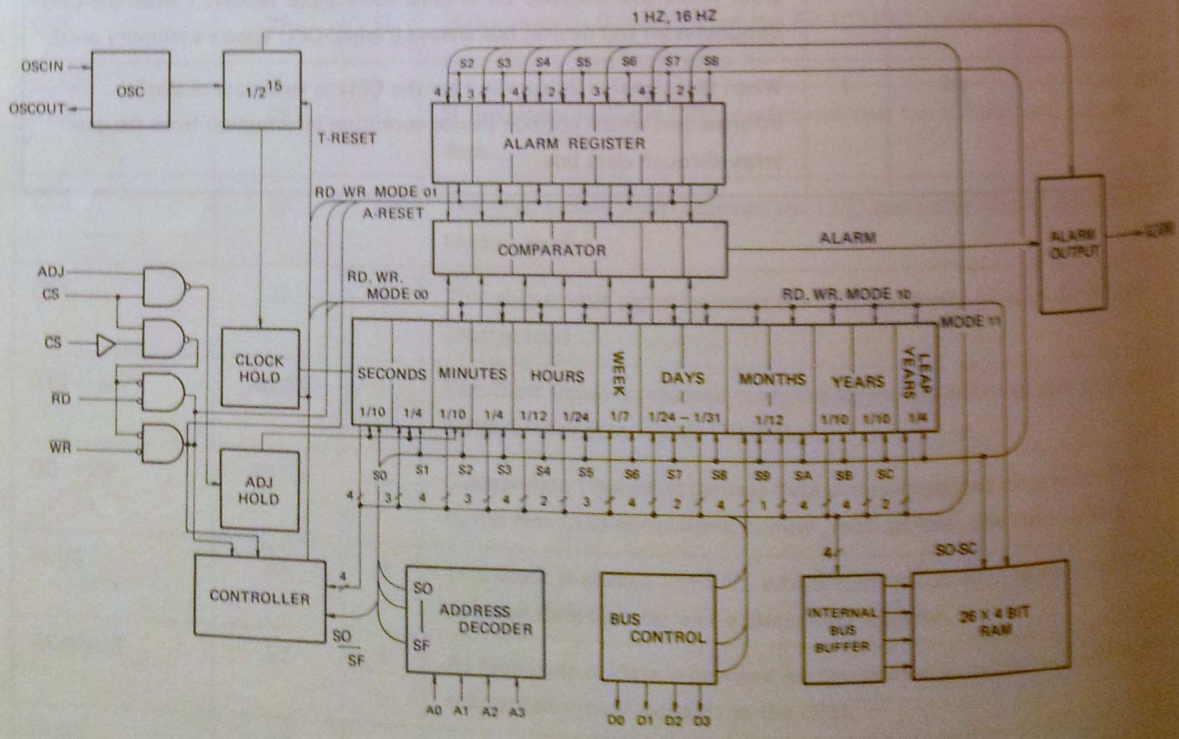


Fig. 6-9 BLOCK DIAGRAM OF TIMER

SIGNAL NAME	I/O	DESCRIPTION
$\overline{CS}$, CS	I	Both input signals are chip-select signals, which are used to select this device. Port $\overline{CS}$ (active low) interfaces the CPU and this device; port CS (active high) is connected to the power-down detector circuit (RESET circuit) to initialize the count when the power voltage becomes low and there is not enough power for all components.
A0 – A3	I	The 4-bit address bus supplied by the CPU can designate 16 address (0-F).
$\overline{RD}$	I	The read enable signal is from the CPU and is used by the CPU to read time and calendar data when it is 0.
$\overline{WR}$	I	Write enable signal. This signal is also from the CPU and is used by the CPU to write data that sets starting time.
D0 – D3	I/O	Bidirectional data bus. These data bus lines are connected directly to the CPU.
OSCIN, OSCOUT	I/O	Terminals to connect crystal oscillator. Clock frequency is 32.768 KHz.
Vcc	I	DC +5 V

Note: All functions not used in the FP-200 are omitted.

OPERATION TIME CHART

WRITE CYCLE (CS = "H")

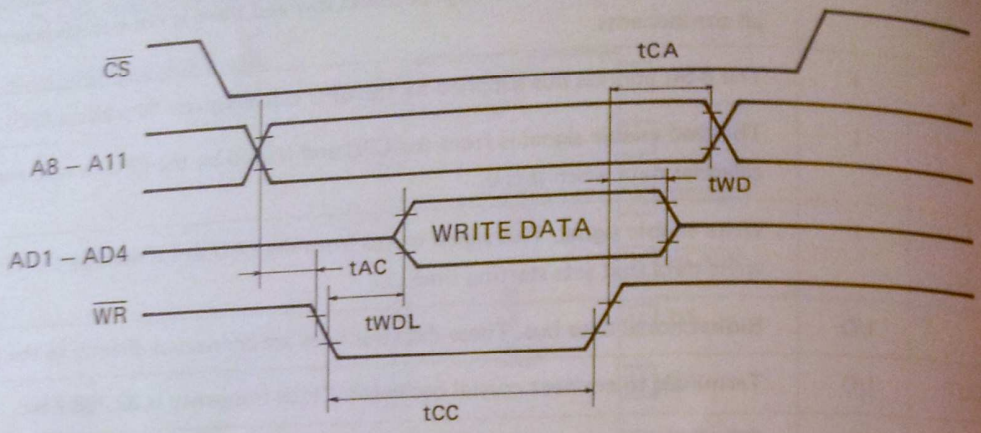


Fig. 6-10 WRITE OPERATION TIMING CHART

READ CYCLE (CS = "H")

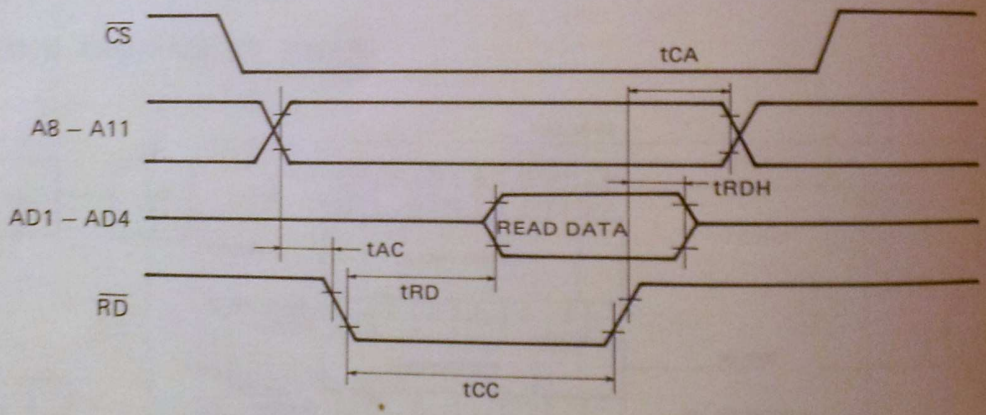


Fig. 6-11 READ OPERATION TIMING CHART

6-4. MEMORY INTERFACE

The circuit below can access, by enabling $\overline{CE1}$ and $\overline{CS}$, the built-in 8K RAM (each RAM has 2K) and a maximum of up to three optional 2K RAM packs or two 2K RAMs and one 8K ROM packs.

When $\overline{WR}$ or $\overline{RD}$ signal is 0 (the CPU can read or write data to memory), the output at inverting NOR gate G2 becomes active and simultaneously pin 3 of J2 is also active (caused by active address A15 and IO/$\overline{M}$ = 0). These two low-active inputs at gate J2 cause the output at pin 6 of the gate to be 0, and $\overline{CE1}$ enables all RAMs of the main memory; it can also enable them through gate E10 if the AUTO-POWER-OFF signal is off (active high) and inverter D10 for decoder H3. In the decoder, timesharingly seven different chip select ($\overline{CS}$) signals for four RAMs of the main memory and three optional memory packs, are output and each chip select signal corresponds to particular address allocation as shown in address table below.

LOCATION: MAIN PCB (P1-1)

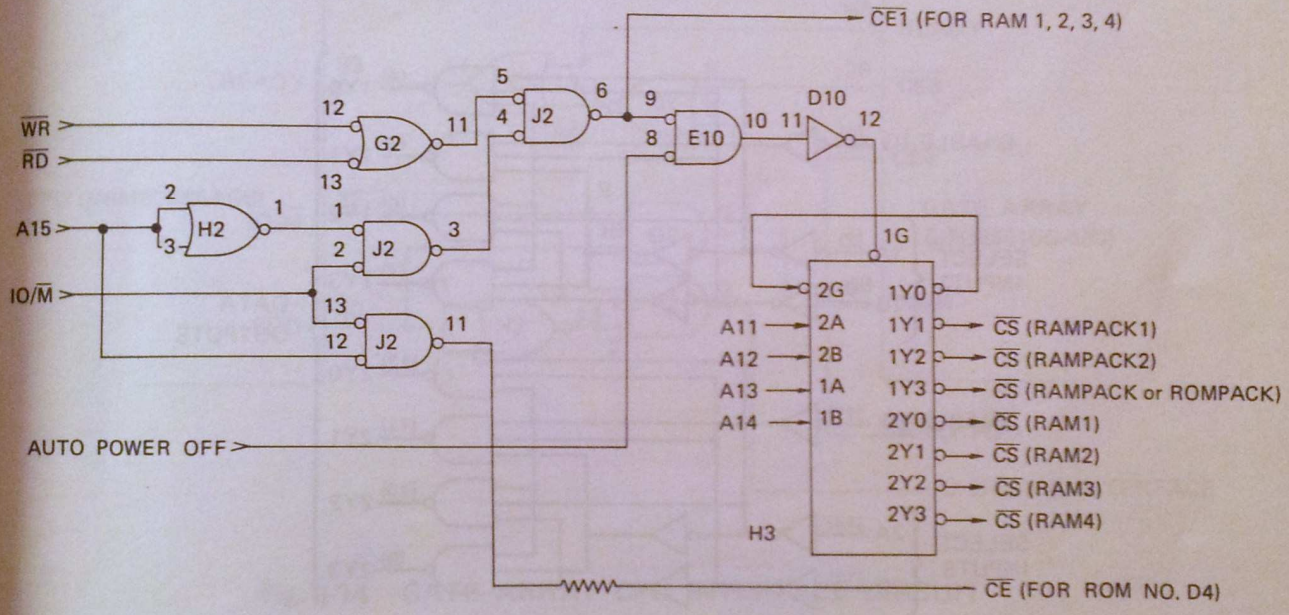


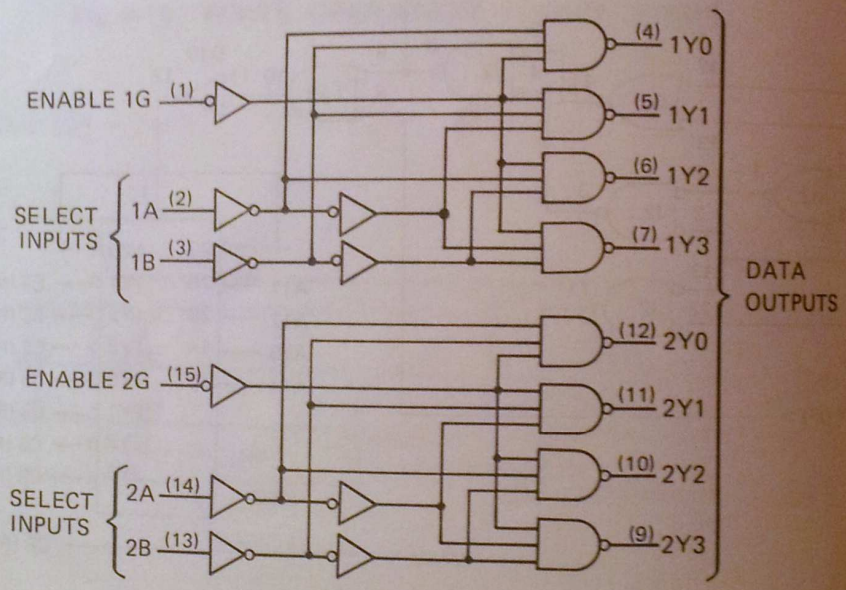
Fig. 6-12 MEMORY INTERFACE CIRCUIT

The memory areas between 8000H and FFFFH, between 32,768 and 65,535, from 0000H to 7FFFH (of 32K memory area) are selected by active or by non active address A15. That is, the ROM contains BASIC and CETL interpreters is selected when A15 is off. Gate J2 makes this possible with low signal of IO/$\overline{M}$ applied at input pin 13. The purpose of AUTO POWER OFF as an input to gate E10 is to protect memory (from destruction or invalid data due to low power). It does this by not letting the enable signal access the decoder H3. Refer to the explanation of AUTO POWER OFF for the theory function of this circuit.

MEMORY ADDRESS ALLOCATION TABLE

ADDRESS	DEVICE	CAPACITY
8000H – 87FFH	MAIN RAM CHIP 1	2K
8800H – 8FFFH	" 2	2K
9000H – 97FFH	" 3	2K
9800H – 9FFFH	" 4	2K
A000H – BFFFH	OPTIONAL RAM PACK 1	8K
C000H – DFFFH	" 2	8K
E000H – FFFFH	" 3 OR ROM PACK	8K

SN74LS139N (IC NO. H3) CIRCUIT DIAGRAM AND TRUTH TABLE



INPUTS			OUTPUTS			
ENABLE G	SELECT B	SELECT A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

Fig. 6-13 CIRCUIT DIAGRAM AND TRUTH TABLE FOR SN74LS139N

6-5. GATE ARRAY (CPU INTERFACE)

Two ready signals, output from the gate array to the CPU, report the ready status. However, the output from pin 62 informs the CPU of the ready status in the control circuit of the gate array and the output from pin 29 declares the ready status in a peripheral device (such as a printer or mini-plotter).

The ready signal from pin 29 is NORed with the high-active IO/$\overline{M}$ signal to assume that the ready signal is generated only when the CPU accesses an I/O address.

AND gate G2 allows the CPU to access the gate array while both inputs (IO/$\overline{M}$ and SOD) are 1; the two H2 gates allow the CPU to access an I/O device while IO/$\overline{M}$ is 1 and SOD is 0.

In other words, gates H2s and G2 switch over between I/O addresses when SOD changes from 1 to 0. When output from SOD is 1, the I/O address map of left half on page 6 is chosen; when it is 0, the address map of right half is chosen.

LOCATION: MAIN PCB (P1-1)

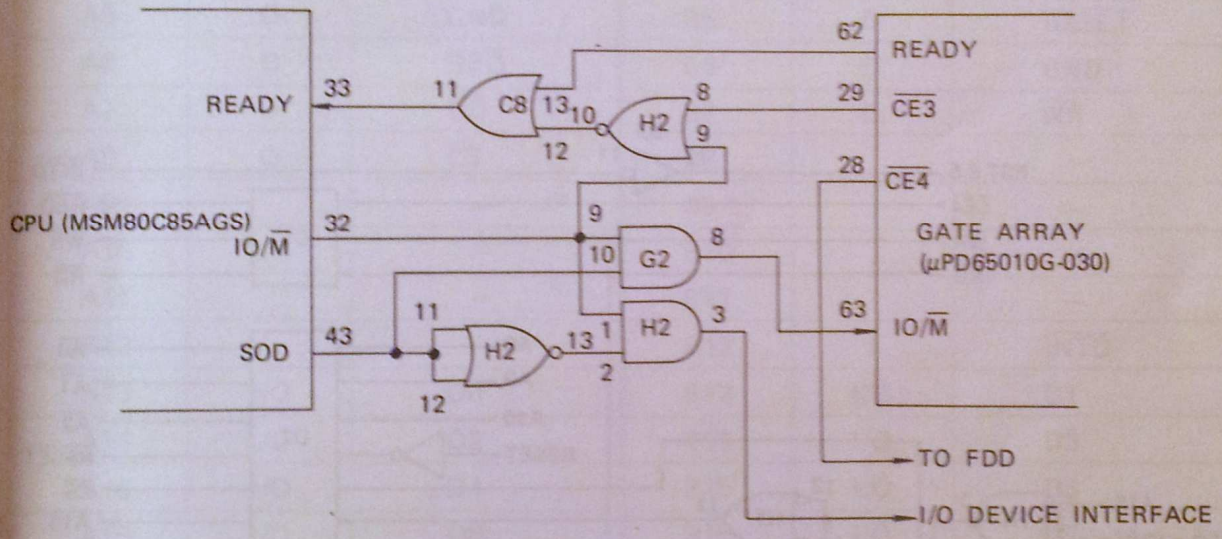


Fig. 6-14 GATE ARRAY CPU INTERFACE CIRCUIT

6-6. FDD INTERFACE

The following circuit is the interface for data and control signals between the gate array in the FDD model FP-1021FD.
Address A15 is used for various accessing and enabling controls in the FDD. First A15 is NAND-ed with SOD•IO/$\overline{M}$ at gate H1. The A15 signal passes through the gate only when the condition is met. Then the signal is inverted by the gate H1.
Two other H1 gates and gate G3 apply the enable signal at buffer gates D2 and C2. Input at pin 4 of first gate H1 allows FDD operations in I/O address 80-8FH, and input pin 5 allows the CPU to read the allocated device code in the FDD at I/O address 40-4FH. The second NAND gate H1 assumes that buffers D2 and C2 pass data only when the CPU reads data from the FDD.
Signal S1 (active low) indicates the operating status of the CPU and lets buffers C1 and C3 pass data from the CPU to the FDD (refer to function description for the CPU on page 13).
C1, D2, D3, D1 and D2 are bus buffer ICs.

LOCATION: MAIN PCB (P1-1)

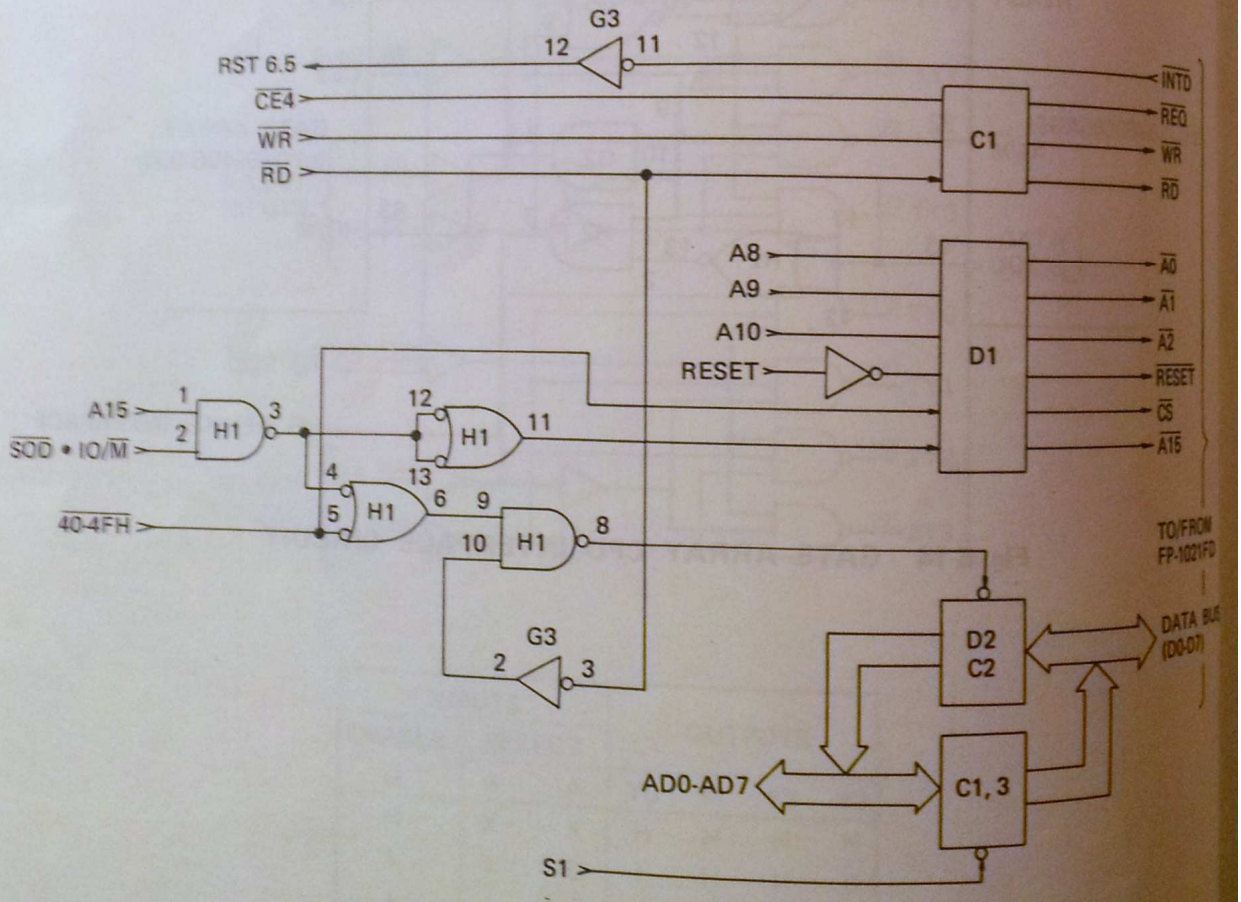
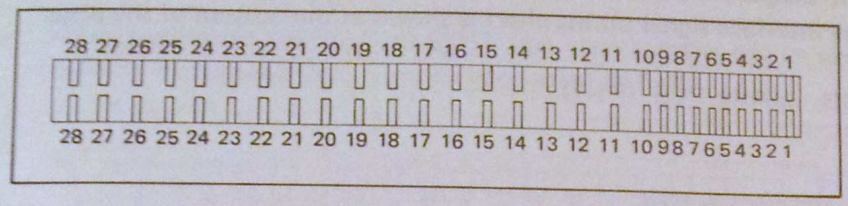


Fig. 6-15 FDD INTERFACE CIRCUIT

FDD CONNECTOR CONFIGURATION



PIN NO.	IN/OUT	SIGNAL NAME	PIN NO.	IN/OUT	SIGNAL NAME
A1		–	B1	O	GND
A2		–	B2	O	GND
A3		–	B3		–
A4	O	GND	B4		–
A5	O	GND	B5	O	$\overline{\text{RESET}}$
A6	O	$\overline{\text{REQ}}$	B6	O	GND
A7	O	$\overline{\text{RD}}$	B7	O	$\overline{\text{WR}}$
A8	O	$\overline{\text{CS}}$	B8		–
A9		–	B9		–
A10		–	B10		–
A11		–	B11		–
A12		–	B12	I	$\overline{\text{INTD}}$
A13	I/O	D0	B13	I/O	D1
A14	I/O	D2	B14	I/O	D3
A15	I/O	D4	B15	I/O	D5
A16	I/O	D6	B16	I/O	D7
A17	O	$\overline{\text{A0}}$	B17	O	$\overline{\text{A1}}$
A18	I/O	$\overline{\text{A2}}$	B18	O	GND
A19	O	GND	B19	O	GND
A20	O	GND	B20	O	GND
A21	O	GND	B21	O	GND
A22	O	GND	B22	O	GND
A23	O	GND	B23	O	GND
A24	O	GND	B24	O	$\overline{\text{A15}}$
A25		–	B25		–
A26		–	B26	O	GND
A27		–	B27	O	GND
A28		–	B28		–

"–" indicates that the pin is not used.

6-7. PRINTER/MINI-PLOTTER INTERFACE

The circuit diagram below is the interface circuit for Centronics-compatible printer or plotter; the interface signal timing chart is shown at the bottom of the page.

LOCATION: MAIN PCB (P1-1)

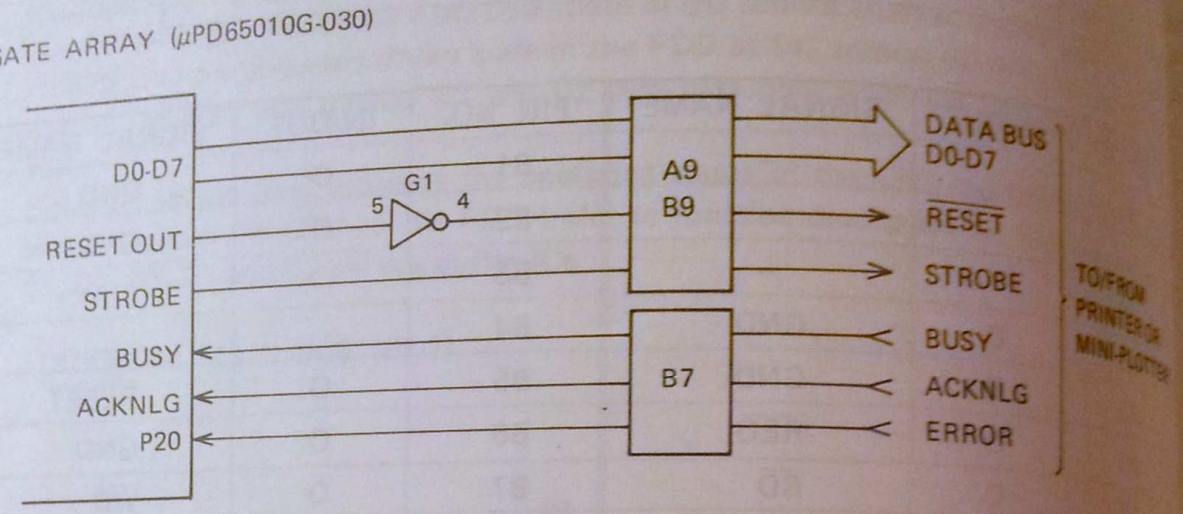


Fig. 6-16 PRINTER/MINI-PLOTTER INTERFACE CIRCUIT

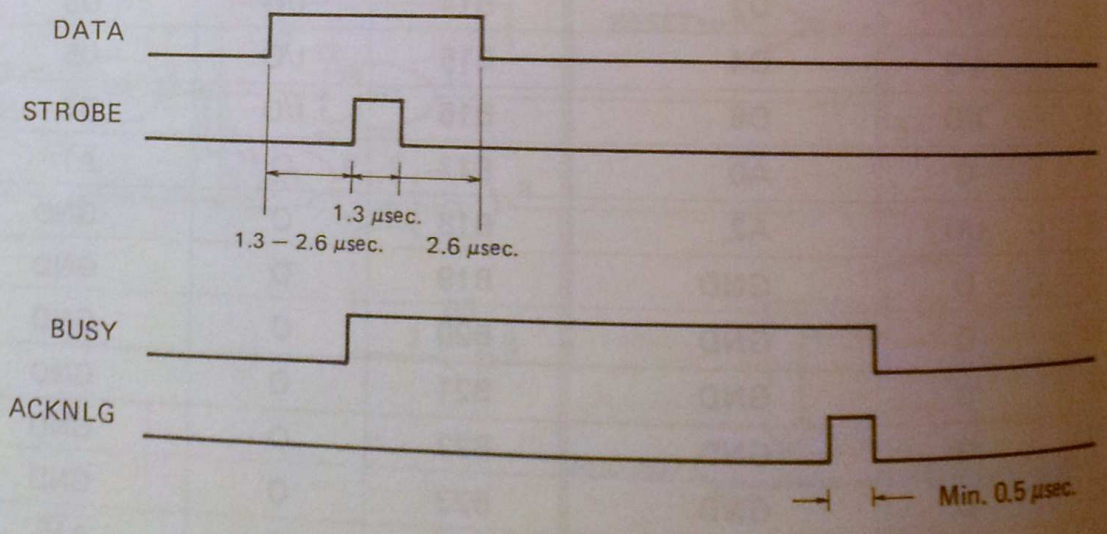
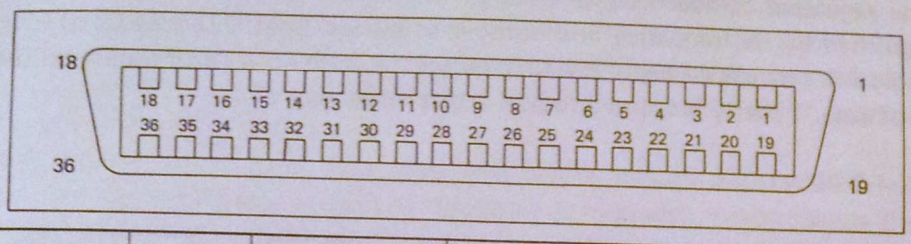


Fig. 6-17 INTERFACE TIMING CHART

Note: Without using the ACKNLG or BUSY line, data transfer can be executed. However, the unused lines must be connected to GND.



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	$\overline{\text{STROBE}}$	19		GND
2	O	DATA1	20		GND
3	O	DATA2	21		GND
4	O	DATA3	22		GND
5	O	DATA4	23		GND
6	O	DATA5	24		GND
7	O	DATA6	25		GND
8	O	DATA7	26		GND
9	O	DATA8	27		GND
10	I	ACKNLG	28		GND
11	I	BUSY	29		GND
12			30		GND
13			31	O	$\overline{\text{RESET}}$
14			32	I	ERROR
15			33		GND
16		GND	34		
17		FG	35		
18			36		

6-8. CMT INTERFACE

The CMT interface in this model is compatible with the "Kansas City standard," used in computer hardware applications. This standard regulates the principles of data recording commercially sold cassette tape with using a commercially sold cassette tape player. Typical regulated standard signal used in this model is shown below. Bit "0" or "1" is distinguished by its frequency and number of pulses. Logical 0 consists of four 1.2-KHz pulses and logical 1 consists of eight 2.4-KHz pulses. (A byte consists of a start bit (always logical 0), 8 bits of data, 1 parity bit, and 2 logical 1 bits respectively.

DATA FORMAT

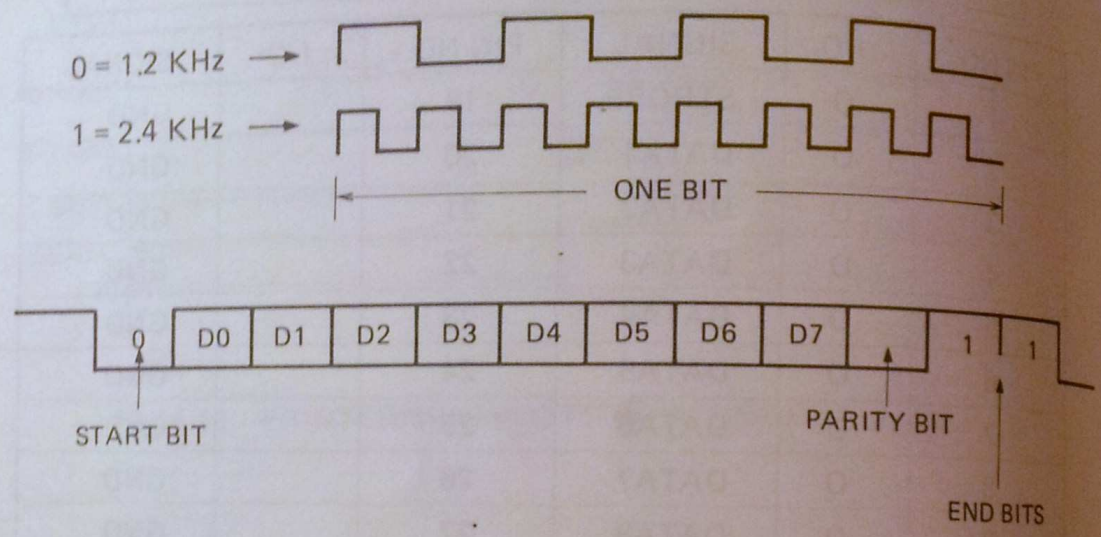
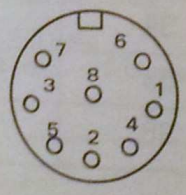


Fig. 6-18 DATA FORMAT

CMT CONNECTOR CONFIGURATION



DIN 8 PIN

PIN NO.	I/O	SIGNAL
1		
2		GND
3		
4	O	MIC
5	I	EAR
6		REM+
7		REM–
8		
CASE		FG

MIC TERMINAL	OUTPUT IMPEDANCE	5 KΩ
	OUTPUT VOLTAGE	3 mVp-p
EAR TERMINAL	INPUT IMPEDANCE	10 KΩ
	INPUT VOLTAGE	3 – 10 Vp-p
REMOTE		24 V, 1 A

6-9. REMOTE CONTROL CIRCUIT

The model FP-200 has an auto start-stop tape player function which turns the motor on or off for read/write operation in CMT.

The function switching the relay switch on-off to power a cassette player's motor is controlled in software as CMT mode is selected, and is stopped automatically when it ends.

As CMT mode is selected and while the power-down detector is not active (it goes low if the power supply voltage becomes abnormally low), transfer data from the gate array is input to AND gate G2 pin 4 through inverter G1 and high level signal of RMT is input to the other terminal to active the AND gate.

Two diodes form a wired AND logic gate, that is the voltage drop at both cathodes is high then output of the AND gate at base of transistor is high also, which causes the transistor to turn on, and causes current to flow through the coil of the relay switch then through the collector-emitter of the transistor.

As current flows, magnetism is generated in the coil, which closes the terminals REM+ and REM−. This shorting condition is held as long as P1 and RMT are 1.

However the relay switch is released if the remote on-off switch on the keyboard is turned off. This causes a low voltage (GND) to be applied to the base of the transistor. If a low power supply voltage is detected, the AND function is turned off (not satisfied).

LOCATION: MAIN PCB (P1-1)

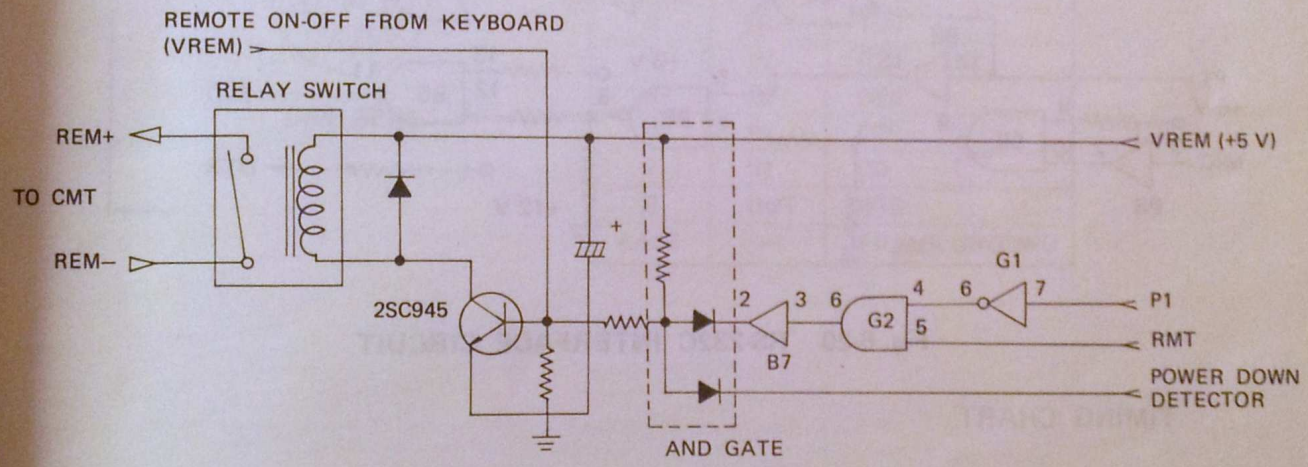


Fig. 6-19 REMOTE CONTROL CIRCUIT

6-10. RS-232C INTERFACE

The FP-200 can communicate with other computers through modems. Serial data at a fixed rate of 300 baud is sent by the half-duplex asynchronous (or synchronous) mode.
In the receive mode, the output of invert NAND gate C8 pin 3 is input to the gate array pin P0; this signal declares that the other side of the communication line is ready to receive data. Incoming serial data is input to $\overline{RxD}$ and is input via the EAR terminal of the gate array. In the output mode, the RTS signal first confirms that the device at the other end is ready; the response is sent back from CTS terminal. When CTS (OSR•CTS) is returned, serial output data is transferred from NAND gate B6 pin 11 through the $\overline{TxD}$ line.

LOCATION: MAIN PCB (P1-1)

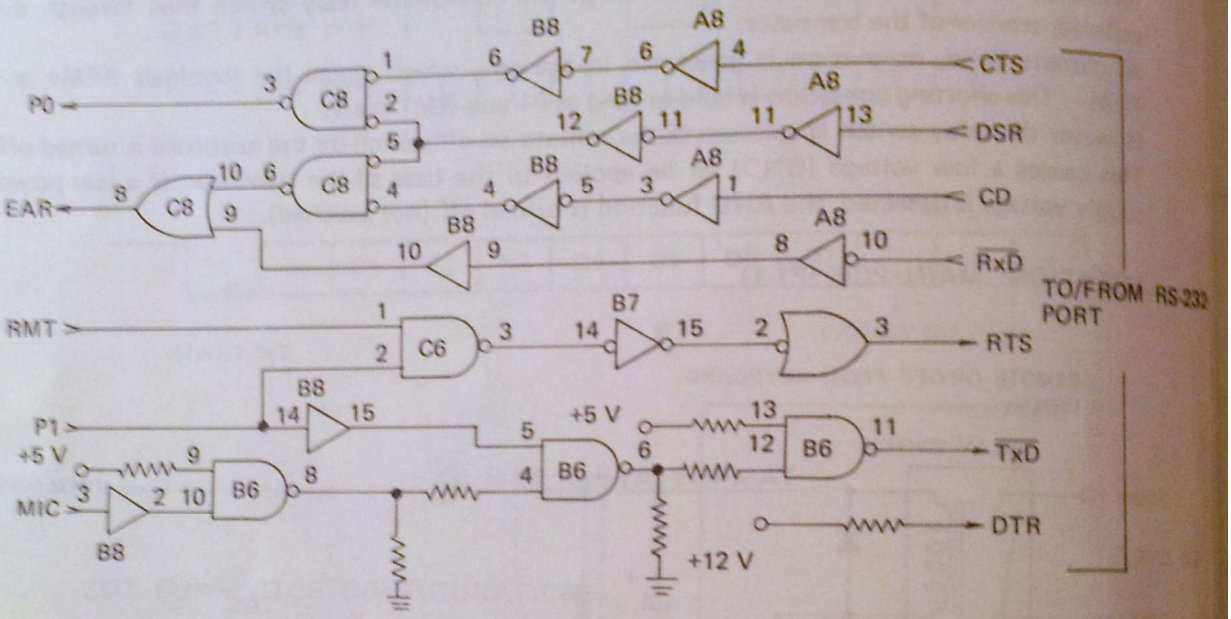


Fig. 6-20 RS-232C INTERFACE CIRCUIT

TIMING CHART

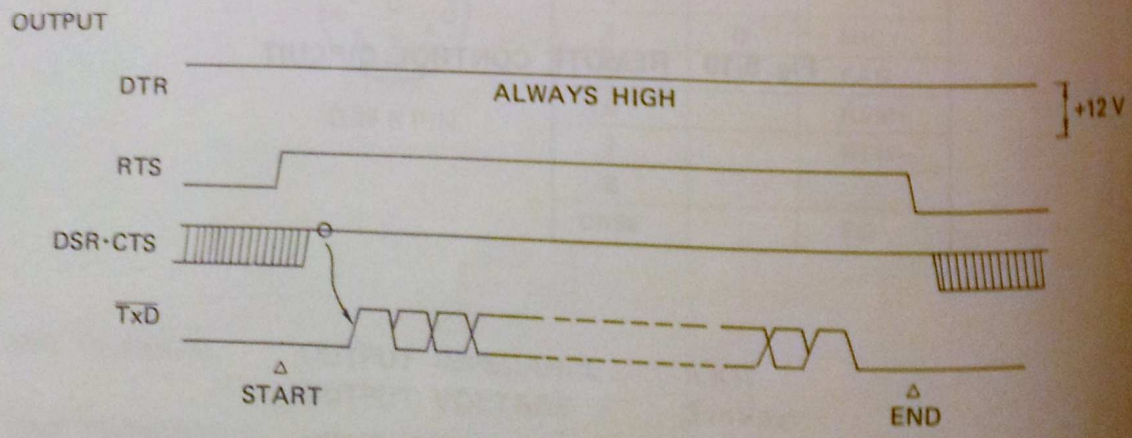
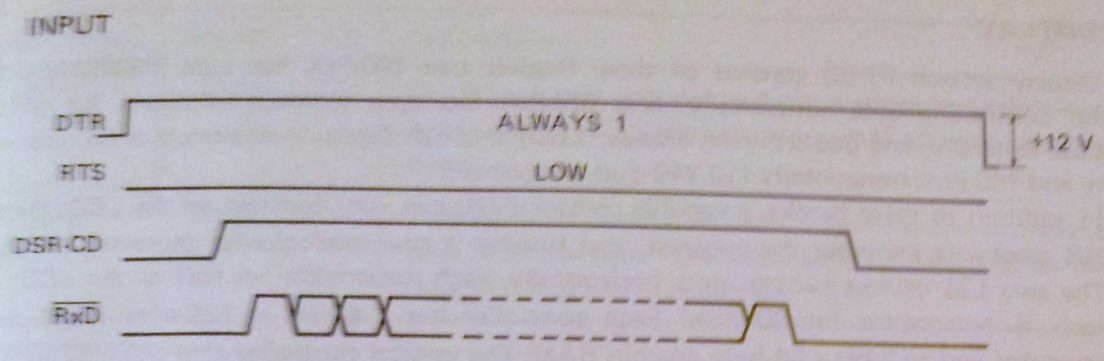


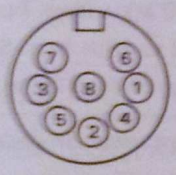
Fig. 6-21 SIGNAL TIMING CHART FOR OUTPUT MODE



Note: Input data is valid only when DSR·CD is 1.

Fig. 6-22 SIGNAL TIMING CHART FOR INPUT MODE

RS-232C PORT CONNECTOR CONFIGURATION



DIN 8PIN

1	OUT	DTR
2	–	GND
3	OUT	$\overline{\text{TxD}}$
4	IN	$\overline{\text{RxD}}$
5	IN	DSR
6	IN	CTS
7	IN	CD
8	OUT	RTS
CASE	–	FRAME GROUND

6-11. DISPLAY

Display section P1-E2 consists of three blocks: two 100-PIN flat type MSM6216-01GS-K for controlling dots horizontally, one 100-PIN flat type MSM6215-01GS-K for controlling dots vertically, and liquid crystal display (LCD) that can display a maximum of 64 dots vertically and 160 dots horizontally (10,240 dots altogether).

In addition to these blocks, a variable resistor (VR) can vary contrast on the LCD; turning the VR clockwise increases the contrast, and turning it counterclockwise decreases the contrast. The two LSI devices control dots horizontally, each responsible for half of the LCD; that is, each is responsible for 80 dots. Each controller has a 64-bit x 128-byte ROM character generator and an 8-bit x 64-byte on-chip RAM. The vertical controller chip (MSM6215-01GS-K) controls dots vertically and can also control the two horizontal controllers.

SIGNAL NAME AND DESCRIPTION

HORIZONTAL CONTROLLER CHIP (MSM6216-01GS-1K, 2 DEVICES)

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
Y1 – Y80 (OR Y81 – 160)	1-13, 51-100	O	Each address signal designates a dot, its location corresponding to its horizontal position. Signals Y1-Y80 are output from the left half of the two controllers and control the 1st to 80th dots. Signals Y81-Y160 are output from the right half and control the 81st to 160th dots.
D1 – D4	47-50	I/O	A 4-bit data bus transfers control information data, character data, and status data to or from this LSI chip.
ϕC1, ϕC2	44,45	I	Clocks generated by the gate array are used to synchronize the controller's function with that of the gate array.
CE1 (or CE2)	41	I	Chip select signal. Chip select signal CE1 selects the left controller of the two; CE2 selects the right controller.
V5, V3, V2	36, 37, 38	I	These LCD drive voltages are generated by the multi-comparator (LA5310) and determine the contrast on the LCD.
ϕf, $\overline{\phi hm}$ ϕs1, $\overline{\phi 2}$	32-35	I	Clocks generated by the vertical controller chip for the two horizontal controller chips.
$\overline{OP}$	46	I	An enable signal used for the LCD controllers when the gate array transfers instructions (not just display data) to the horizontal controller chips. It is an active-low signal; instruction data is transferred to the gate array when it is 0.
M1, GND, VDD1, 2	39, 40, 42, 43	–	Signal ground
X1 – X64	48-41, 39-16, 14-1, 83-100	O	This signal specifies a vertical dot address on the LCD.
XOUT, XIN	49, 50	I/O	Connecting terminals for crystal oscillator. In this model, 6.16-MHz clock frequency is input to this controller chip.

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
V5, V4, V1	61-63	I	LCD drive voltages generated by the multi-comparator determine the contrast on the LCD. These voltages are set by adjusting the variable resistor.
ϕ1, ϕhm ϕs1, $\overline{\phi 2}$	59-62	O	These clocks are output from this chip for the two horizontal controller chips for vertical scans. These signals are synchronizing signals which cause horizontal data to be output.

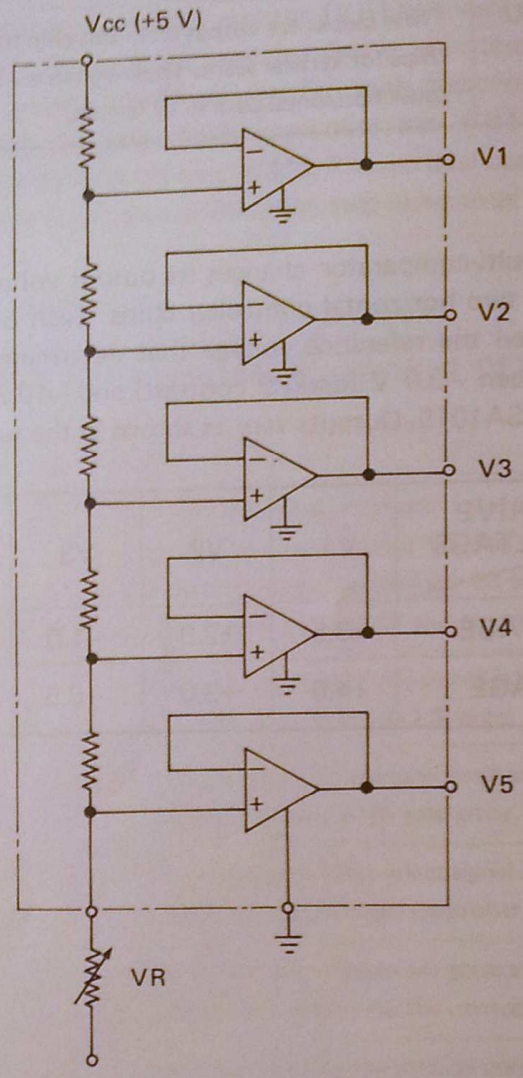
MULTI-COMPARATOR

To change the contrast, the multi-comparator changes its output voltages, which are applied to the vertical controller chip and the two horizontal controller chips. Each output from the comparator is varied within some extent when the reference voltage that determines output level is varied. The reference voltage is varied between −3.0 V (darkest contrast) and −10.2 V (lightest contrast) measured at the emitter of transistor 2SA1015. Outputs vary as shown in the table below.

LEVEL \ LCD DRIVE VOLTAGE	V1	V2	V3	V4	V5
MAXIMUM VOLTAGE	+3.5	+2.0	−1.0	−2.0	−10.0
MINIMUM VOLTAGE	+4.0	+3.0	+0.5	−1.5	−2.5

COMPARATOR EQUIVALENT CIRCUIT

LM5310M



VLCD (−15 V), REFERENCE VOLTAGE

6-12. POWER-DOWN DETECTOR CIRCUIT

To protect contents of main memory from the dangers caused by a low power supply voltage, the circuit shown below provides a reset pulse to stop the CPU when the power (+5 V) goes down below +3.8 V.

When the power is between +5 V and +3.8 V, output from pin 7 of the comparator is about ground level, causing transistor 2SC945 to be off. Therefore, voltage drop at the collector of the transistor is high and consequently output from inverter D10 pin 2 is also high.

Suppose the input voltage is negative (−), pin 6 drops to less than 3.8 V, the output level at pin 7 is reversed − its previously low level is about +5 V. Then the LED is lit and the transistor 2SC945 is turned on causing the output from D10 pin 2 to be low. Thus, pulse length of the

LOCATION: MAIN PCB (P1-1)

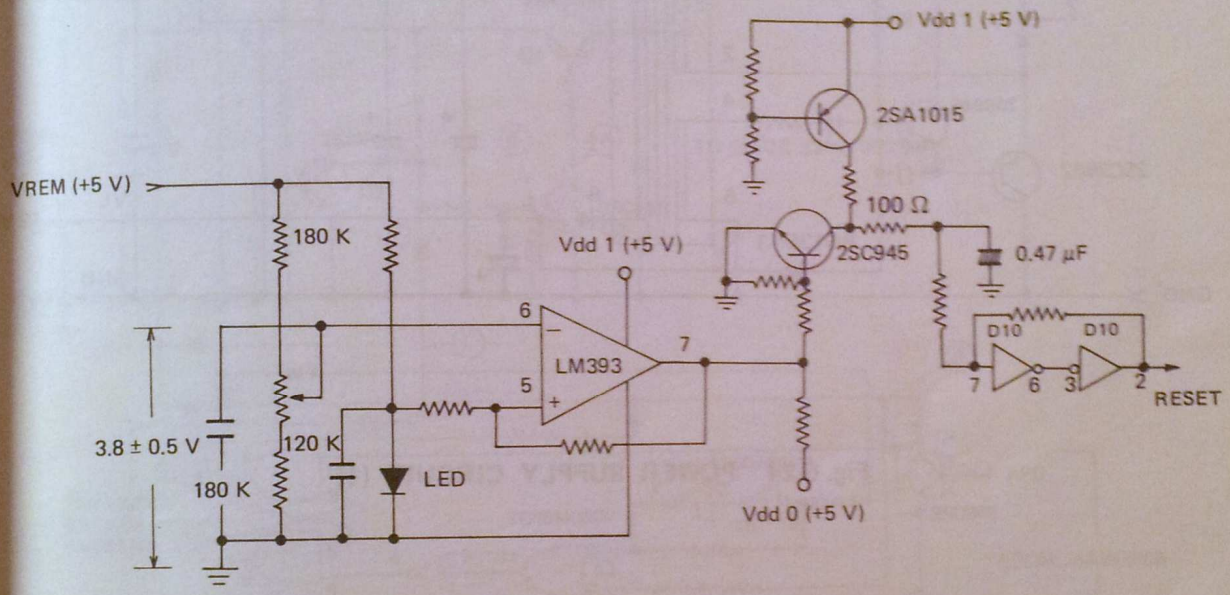


Fig. 6-23 POWER-DOWN DETECTOR CIRCUIT

reset pulse should be equal to three basic clock pulses. The pulse delay causes the reset pulse length to be the three basic clock pulses resulting from the 100 Ω resistor and 0.47 μF electrolytic capacitor, which form an integrating circuit.

The purpose of the reset pulse right after the power-on is not only to initialize the CPU but also to prevent mis-functioning of CMT remote control circuit and LCD display controllers.

Though the voltage drop between pin 6 of the comparator and ground has been set to 3.8 ± 0.5 V by adjusting the variable resistor, in case any of the components connected pins 6 and 5 (including the comparator itself) is replaced, the voltage drop must be confirmed again to see if it is within tolerances.

Two D10s shape up the reset pulse to be exact square wave.

6-14. POWER SUPPLY CIRCUIT (2)

The circuit shown below is mostly on the P1-S1 printed circuit board. The lower portion of the diagram is the auto-power-off circuit.

When battery power is used as main power source, the APO signal (generated by the main PCB when the unit is left on for seven to nine minutes) is applied to the base of transistor 2SC945, causing the collector voltage to drop or the voltage at pin 10 of TC40H000P (F-F gate) to drop to nearly ground level. When this low voltage signal is applied to input pin 10, the F-F gate reverses its output (to high).

LOCATION: POWER SUPPLY PCB (P1-S1)

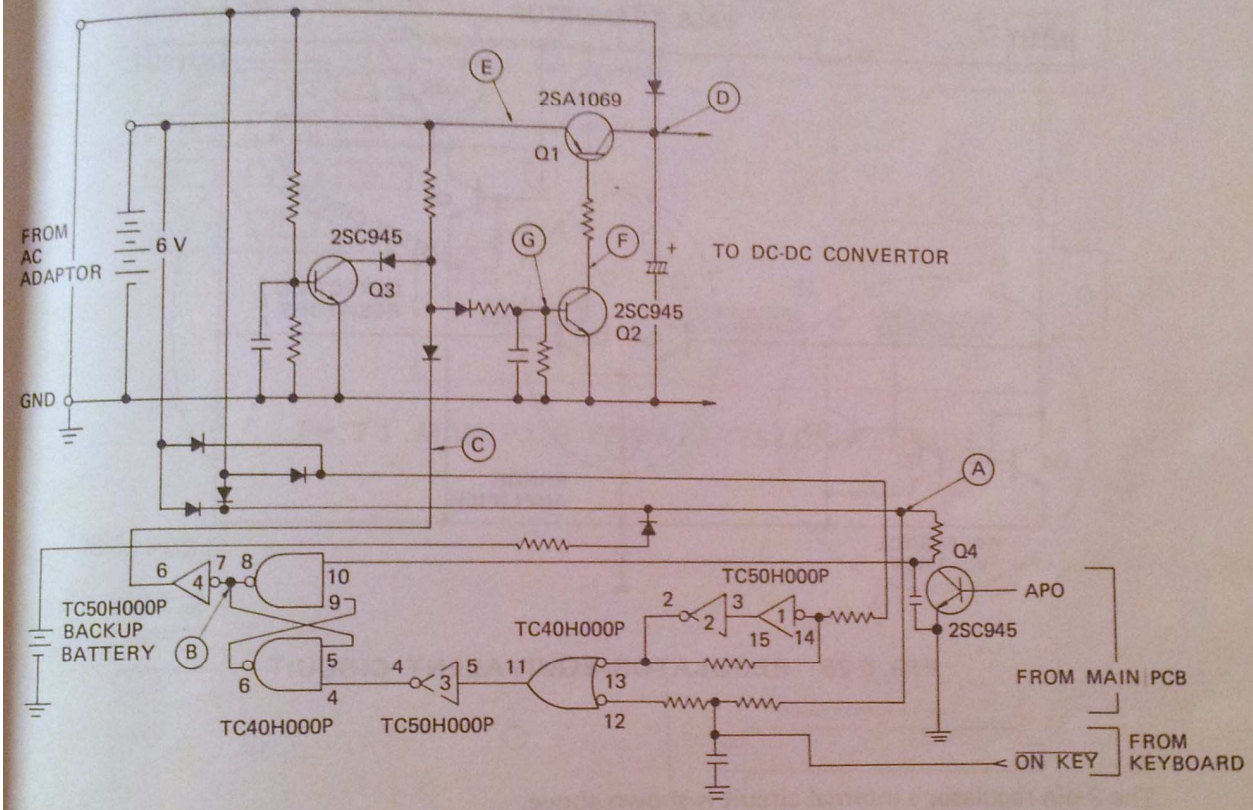


Fig. 6-25 POWER SUPPLY CIRCUIT (2)

The high output is once inverted and becomes low so that voltage drop at base of transistor Q2 is forced low also.

The result causes transistors Q2 and Q1 to go off. Thus, +6 V from the battery cannot be supplied to the oscillation transistors.

The F-F holds its output status until $\overline{\text{ON KEY}}$ signal from the keyboard (active low) is input to pin 4 of the other input. The low input signal reverses the output status of the F-F (to low), causing transistors Q2 and Q1 to turn on.

When the AC adaptor is used as the main power source, the auto-power-off circuit, however since the power voltage is applied after transistor Q1, is useless and the power voltage from the adaptor is supplied to the oscillation transistors.

VOLTAGES AT VARIOUS POINTS

	A	B	C	D	E	F	G
WHEN DISPLAY ALIVE	6.0	0	5.0	6.0	6.0	0	0.7
WHEN MAIN POWER SOURCE ALIVE BUT NO DISPLAY	6.0	5.0	0	0	6.0	5.0	0

3-PIN REGULATOR'S EQUIVALENT CIRCUIT

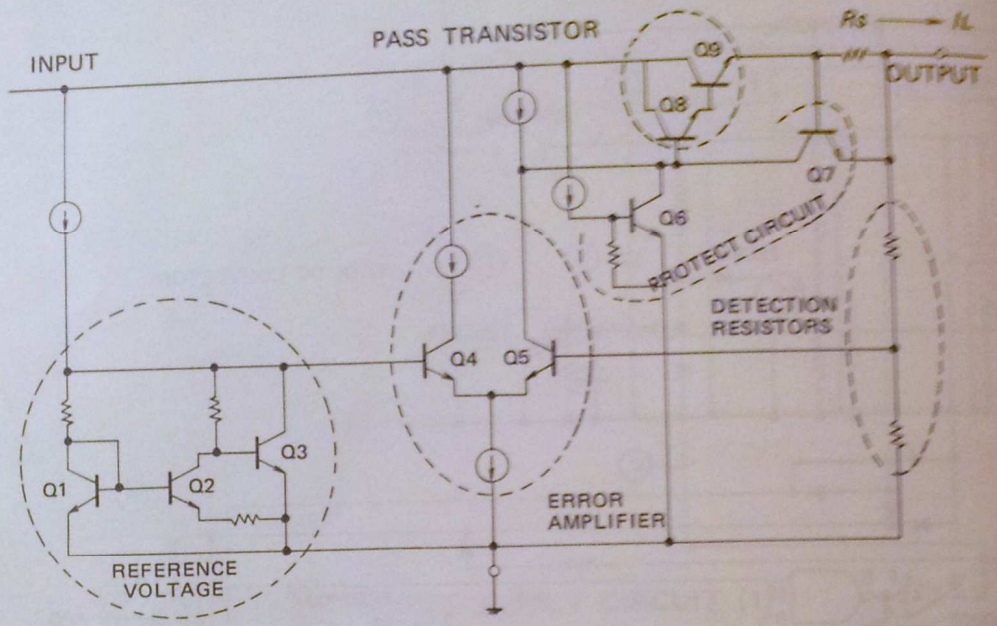


FIG. 6-26 REGULATOR EQUIVALENT CIRCUIT

The 3-pin regulator's internal circuit is shown above.
Transistors Q1-Q3 are band-gap transistors and provide a reference voltage. Accumulated voltag between the emitter and the base is utilized to generate stable voltage with low nois
Transistors Q4 and Q5 form an error amplifier and transistor Q9 (a pass transistor) has it base connected with transistor Q8 to control output voltage.
Transistor Q7 controls current flow on the output line and transistor Q6 is sensitive to tempera ture, detecting abnormal temperatures.
Transistors Q7 and Q6 protect the pass transistor. Transistor Q7 is turned on by an abnorma voltage and current on the output line, and transistor Q6 turns on by an abnormal temperature. They act as a passage gate to cause input flows through Q6 and Q7 instead of Q9.
Thus, the current flowing through the transistor Q9 is shut off and the output is curbed.

7. CIRCUIT DIAGRAMS

COMPONENT LAYOUTS

Main PCB

SIDE 1

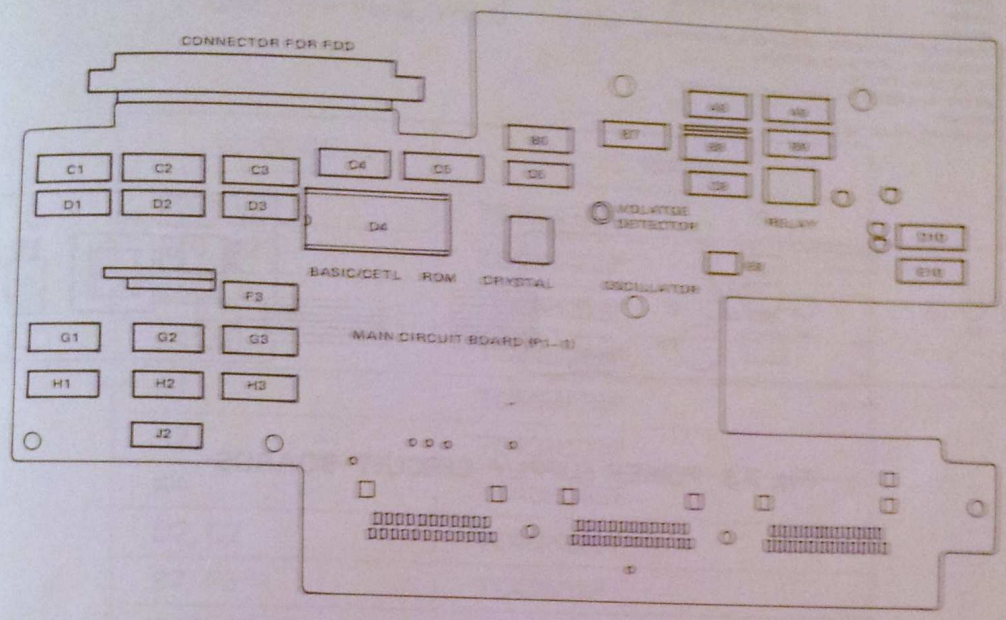


Fig. 7-1 MAIN P.C.B. FROM PARTS-LOCATED SIDE

Main PCB

SIDE 2

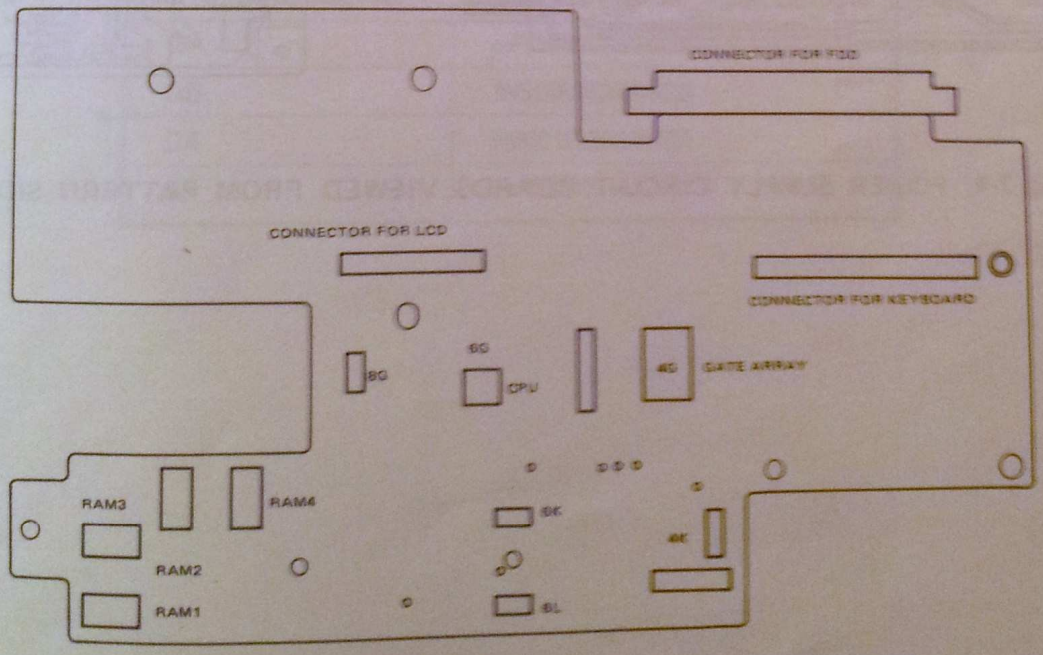


Fig. 7-2 MAIN P.C.B. VIEWED FROM PATTERN SIDE

POWER SUPPLY PCB (P1-S1)

C2 : DC-DC CONVERTER
Q3 : 2SA1069 TRANSISTOR (PASS TRANSISTOR)
Q4 : 2SC945 " (VOLTAGE DETECTOR)
Q5 : 2SC945 " (APO ON-OFF TRANSISTOR)
Q6 : 2SC945 " (VOLTAGE DETECTOR)
Q7 : 2SC945 " (FOR OSCILLATION)
Q8 : 2SD789 " (")
IC2 : TC40H000P IC(INVERT OR GATE & INVERTER)
IC3 : TC30H000P IC(F/F & INVERTER)
C1 : DC-DC CONVERTER
Q1 : 2SC945 TRANSISTOR (FOR OSCILLATION)
Q2 : 2SC2562 " (")
IC1 : 78M05 VOLTAGE REGURATOR

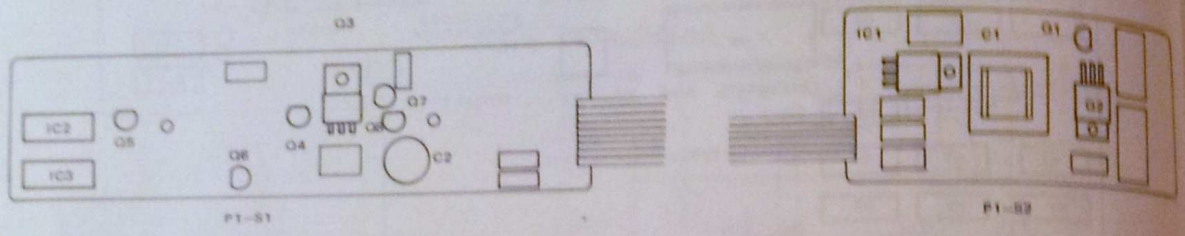


Fig. 7-3 POWER SUPPLY CIRCUIT BOARDS

POWER SUPPLY PCB (P1-S2)

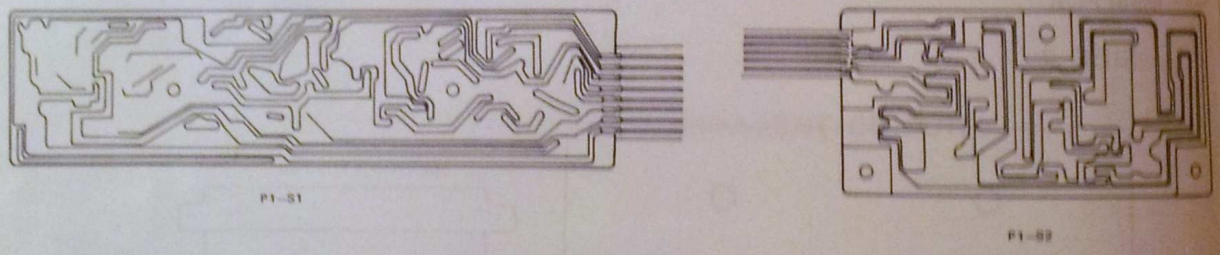
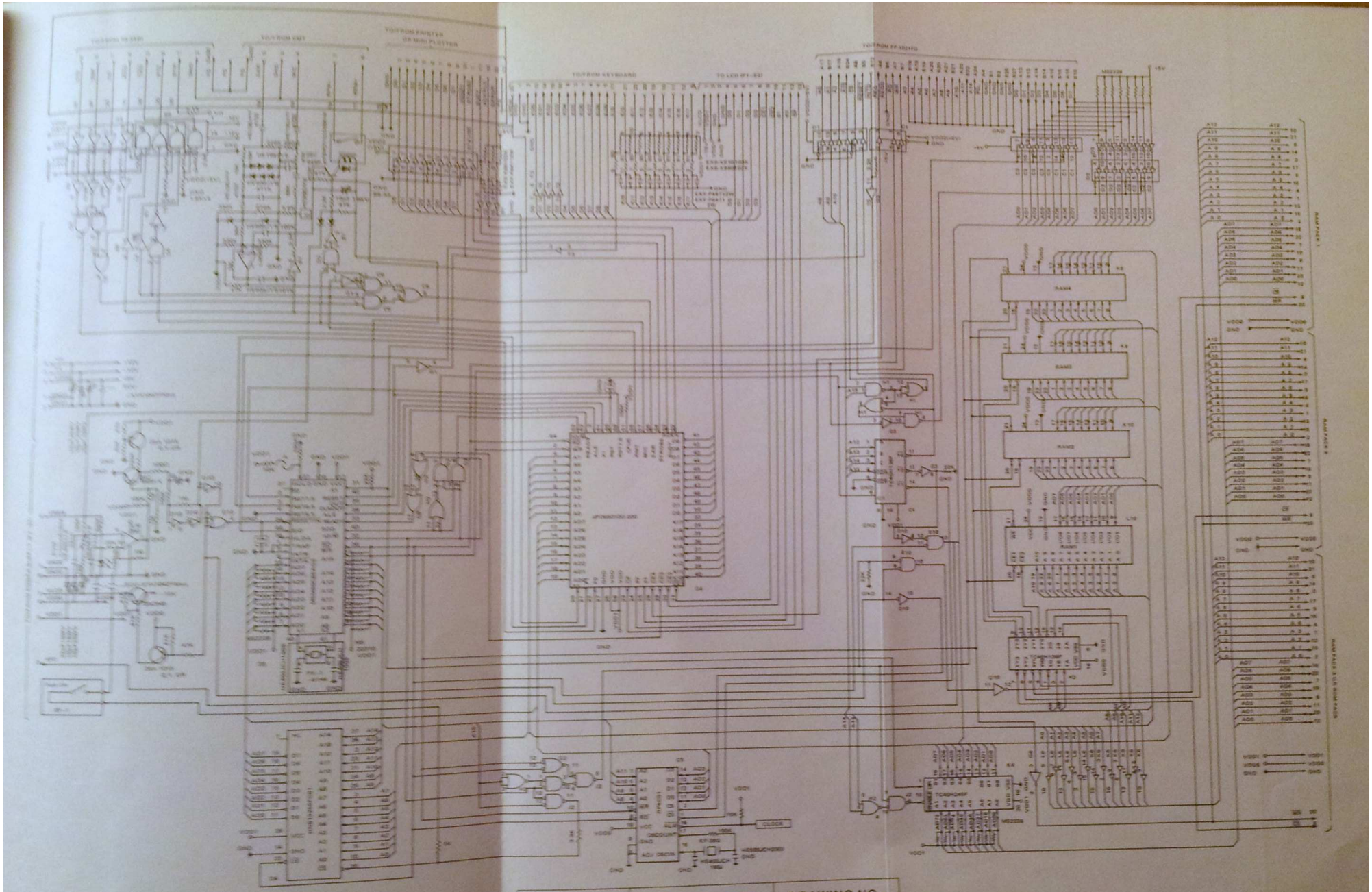


Fig. 7-4 POWER SUPPLY CIRCUIT BOARDS VIEWED FROM PATTERN SIDE

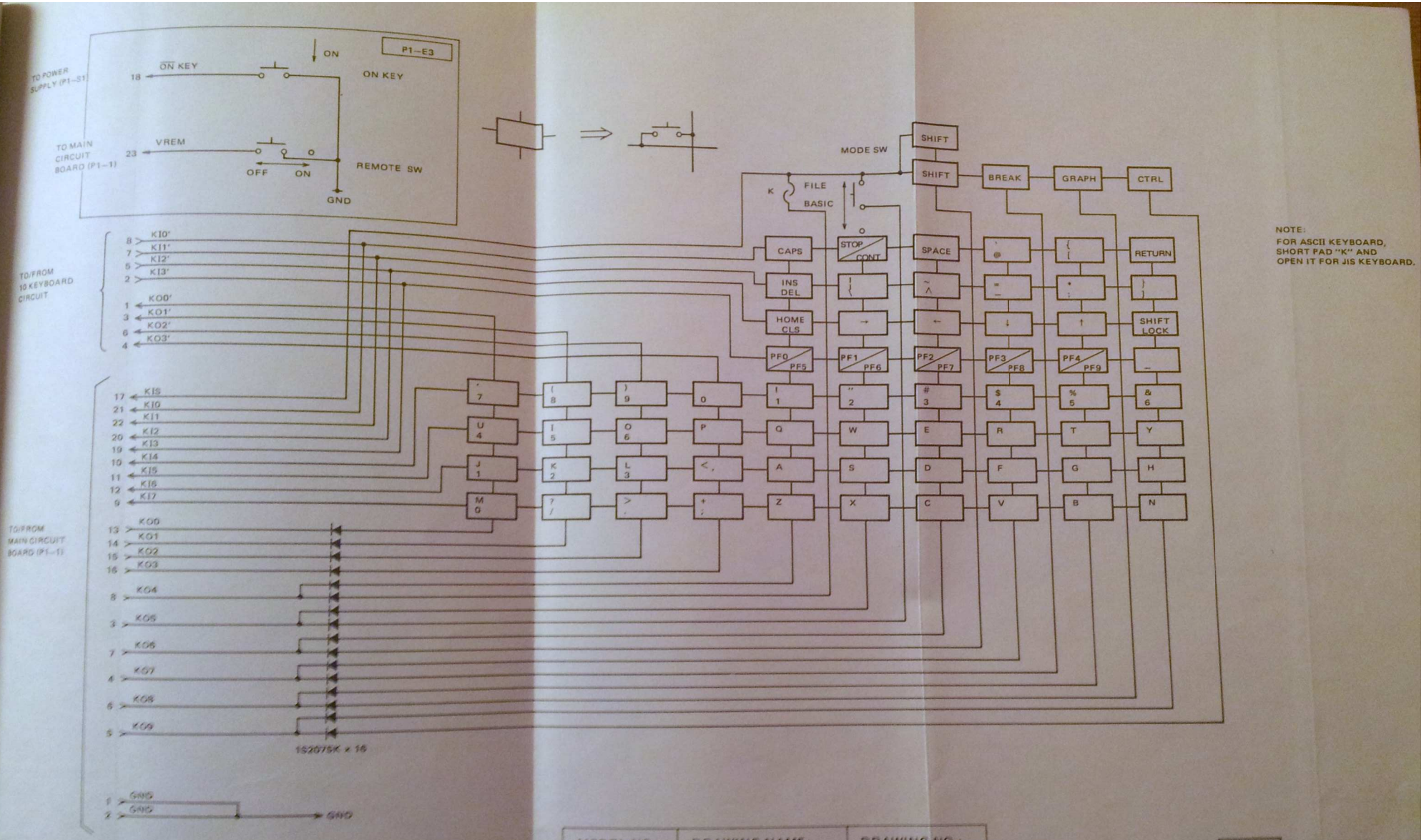
Notes;

1. All resistors without specification printed are ¼ W.
2. All diodes without specification printed are 1S2072K.
3. All voltage without voltage's name is Vdd 1, +5 V.
4. TC40H002P (E10)
   GND ⟶ Pin 7, Vdd 0 ⟶ Pin 14
   TC50H000P (D10)
   GND ⟶ Pin 8, Vdd 0 ⟶ Pin 1

IC CODE	IC NAME
C6, H1	TC40H000P
E10, H2	TC40H002P
G2	TC40H008P
C8, J2	TC40H032P
C4	TC40H138P
H3	TC40H139P
K4	TC40H245F
D2, C2	TC40H368P
B7, F3	TC4050BP
D10, D3, G1, G3	TC50H000P
B8, K6, G8, L6	TC50H001F
B9, A9, D1, C1, C3	SN74LS367AN
B6	SN75188N
A8	SN75189N
L10, K10, K9, K8	μPD449G-1 (or TC5518BF-20)
G4	μPD65010G-030
G6	MSM80C85AGS
D4	HN613256PC01
C5	RP5C01



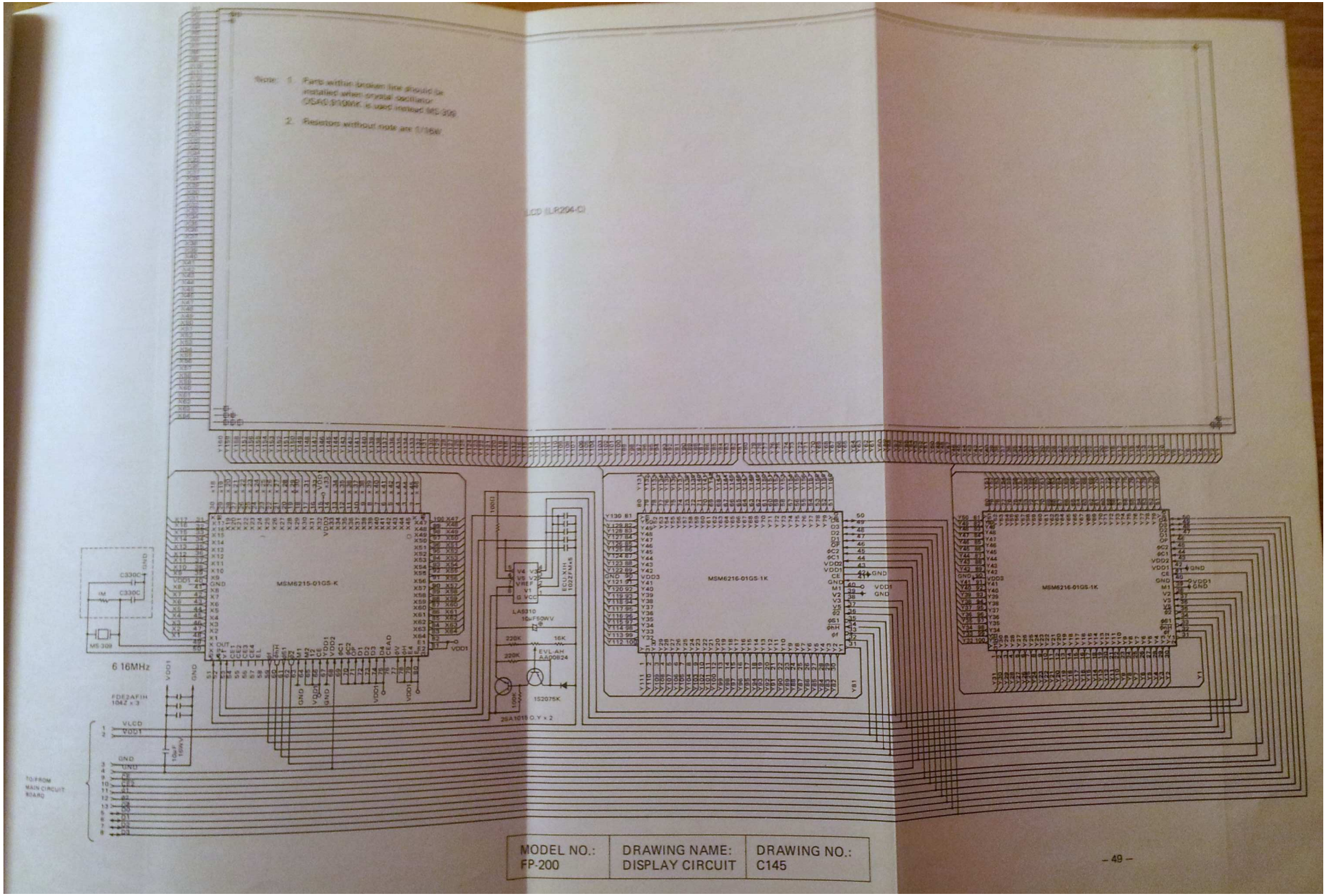
MODEL NO.:	DRAWING NAME:	DRAWING NO.:
FP-200	MAIN CIRCUIT	C141



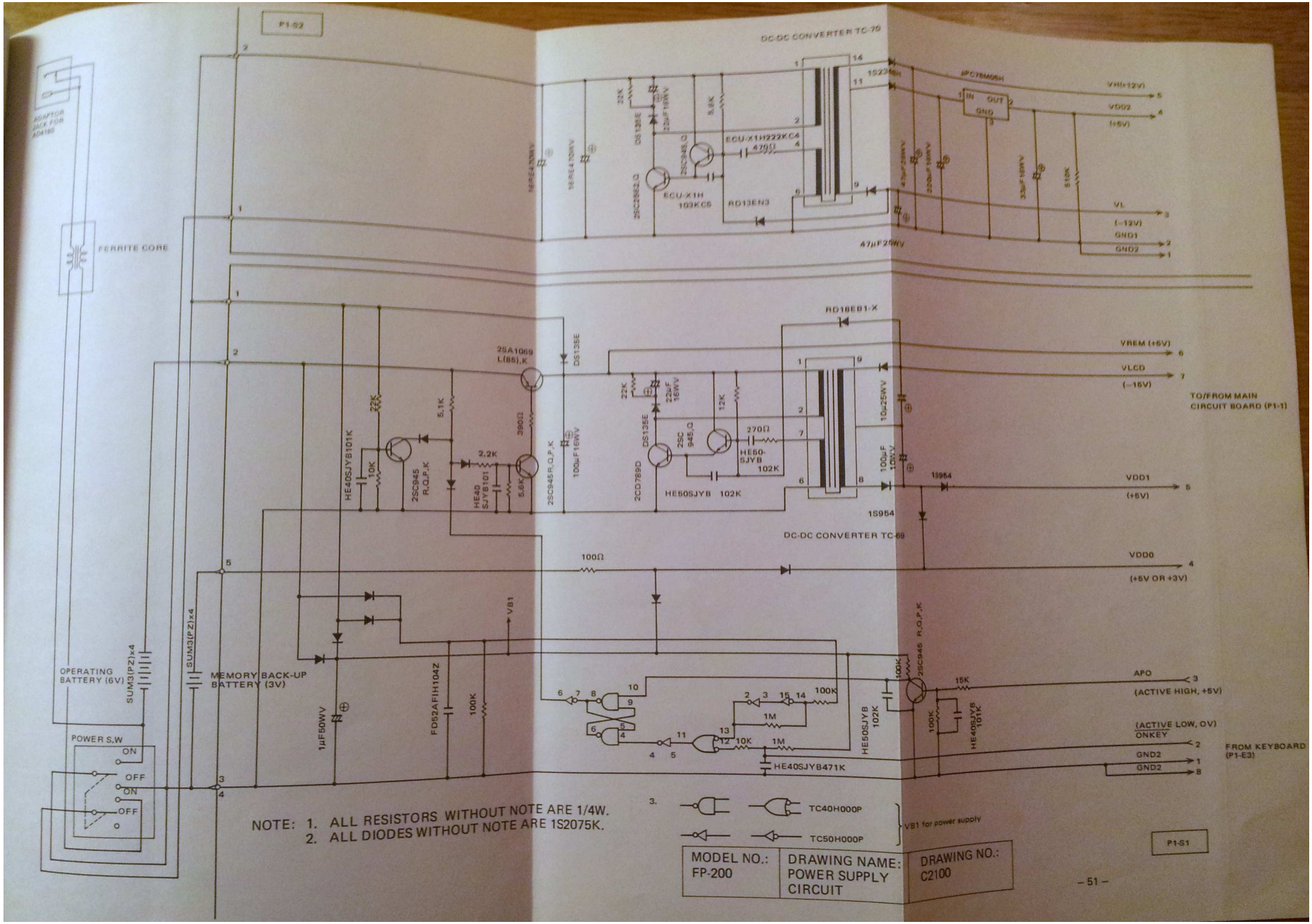
NOTE:
FOR ASCII KEYBOARD, SHORT PAD "K" AND OPEN IT FOR JIS KEYBOARD.

MODEL NO.:	DRAWING NAME:	DRAWING NO.:
FP-200	KEYBOARD CIRCUIT	C299 ASCII

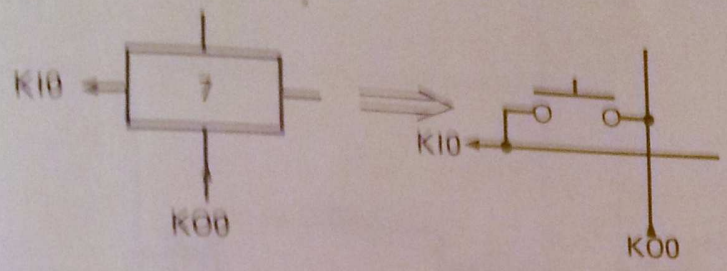
P1—E4

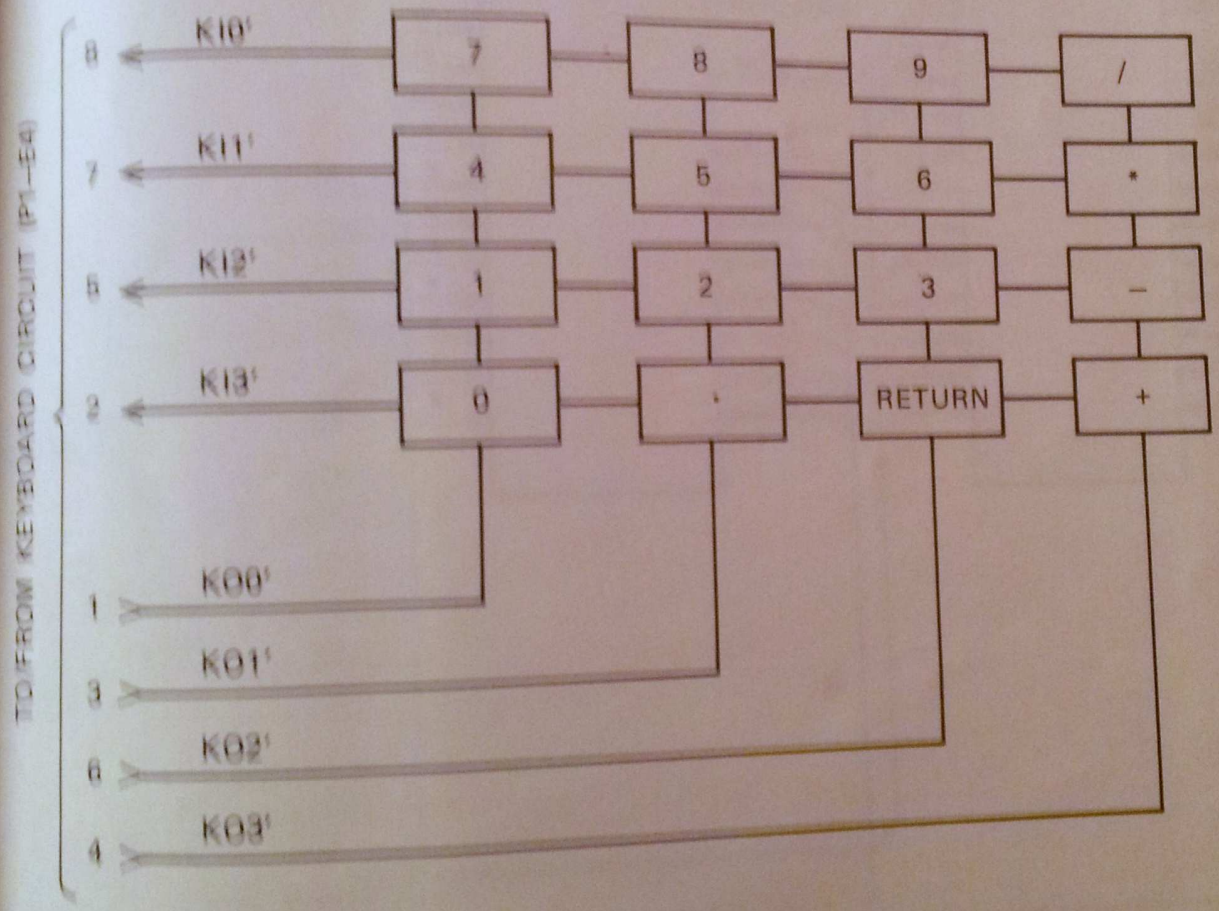


MODEL NO.:	DRAWING NAME:	DRAWING NO.:
FP-200	DISPLAY CIRCUIT	C145

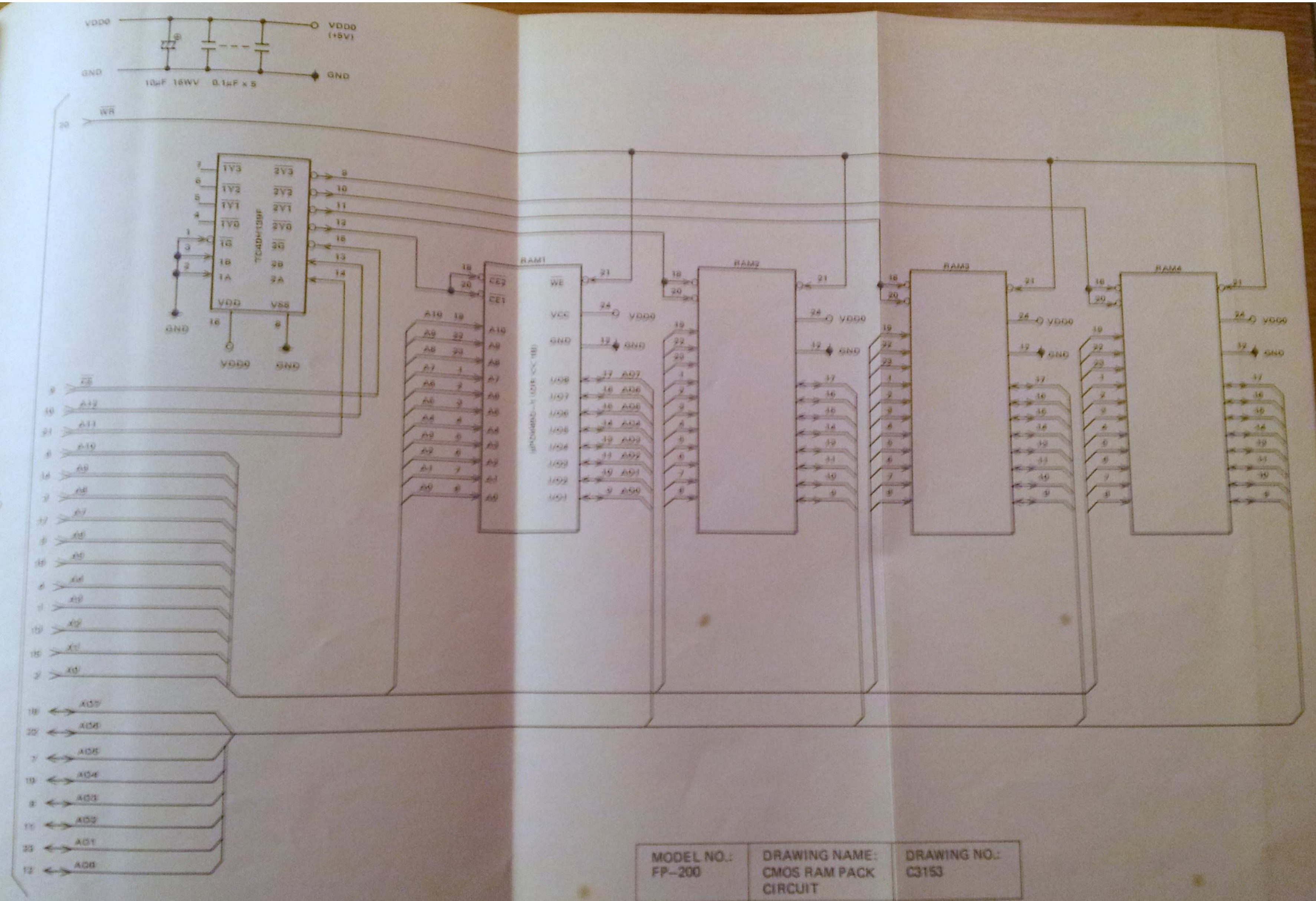

P1-S2
DC-DC CONVERTER TC-70
ADAPTOR JACK FOR AD4160
FERRITE CORE
ECU-X1H222KC4
ECU-X1H 103KC5
RD13EN3
IPC78M05H
VH(+12V)
VDD2 (+5V)
VL (−12V)
GND1
GND2
47μF25WV
RD18EB1-X
VREM (+5V)
VLCD (−15V)
TO/FROM MAIN CIRCUIT BOARD (P1-1)
2SA1069 L(65),K
HE40SJYB101K
2SC945 R,Q,P,K
HE40 SJYB101I
HE50-SJYB 102K
HE50SJYB 102K
2CD789D
DS135E
1S954
VDD1 (+5V)
DC-DC CONVERTER TC-69
100Ω
VDD0 (+5V OR +3V)
VB1
OPERATING BATTERY (6V)
SUM3(PZ)x4
MEMORY BACK-UP BATTERY (3V)
1μF50WV
FD52AFIH104Z
100K
POWER S.W
ON
OFF
HE40SJYB471K
HE50SJYB 102K
HE40SJYB 101K
APO (ACTIVE HIGH, +5V)
(ACTIVE LOW, OV) ONKEY
GND2
FROM KEYBOARD (P1-E3)
3. TC40H000P
TC50H000P
VB1 for power supply
NOTE: 1. ALL RESISTORS WITHOUT NOTE ARE 1/4W.
2. ALL DIODES WITHOUT NOTE ARE 1S2075K.
MODEL NO.: FP-200
DRAWING NAME: POWER SUPPLY CIRCUIT
DRAWING NO.: C2100
P1-S1

EXAMPLE

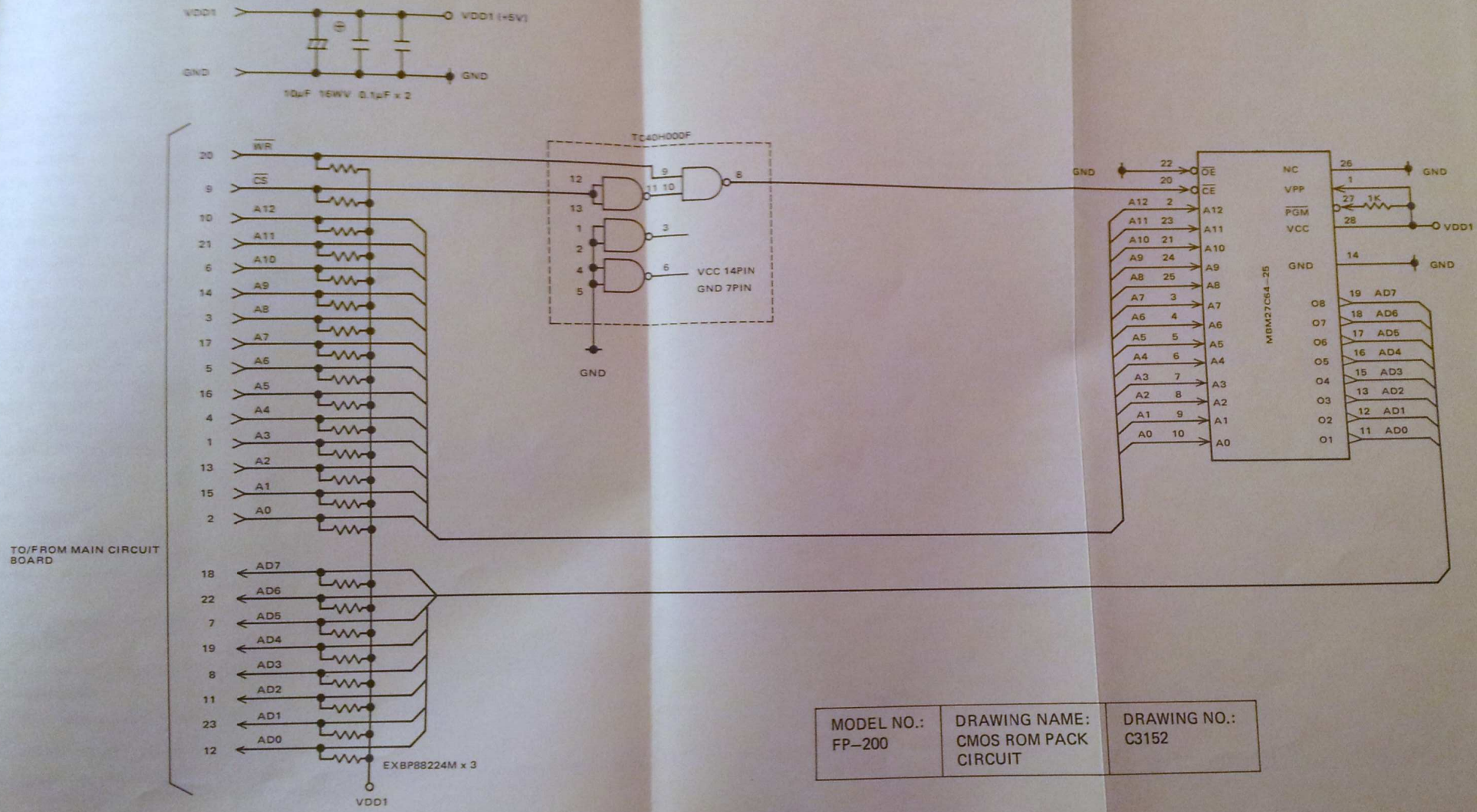




MODEL NO.: FP-200	DRAWING NAME: 10 KEYBOARD CIRCUIT	DRAWING NO.: C4184



MODEL NO.:	DRAWING NAME:	DRAWING NO.:
FP–200	CMOS RAM PACK CIRCUIT	C3153



MODEL NO.:	DRAWING NAME:	DRAWING NO.:
FP–200	CMOS ROM PACK CIRCUIT	C3152

8. TEST PROGRAM

The test program, its file name TP and loaded from the floppy diskette, can diagnose the following internal hardware circuits, components, and peripheral devices that are available to the FP-200. This program ability has, however, limitation to its capability and it cannot detect all kinds of trouble. The program can run under the conditions where the CPU and the gate array function normally, all power voltages are normally provided to all sections, and the FDD interface functions normally.

8-1. MENU

	COMMAND CODE (PROGRAM FILE NAME)
MASK ROM CHECK	
ROM PACK CHECK	MR
DATA WRITE IN RAM PACK	ER
DATA VERIFICATION IN RAM PACK	CW
DATA WRITE CHECK IN RAM PACK	CR
DATA WRITE IN PRINTER	RM
MEMORY DUMP	LP
SETTING AND COUNTING TIME	DM
DISPLAY CHECK	TM
DATA WRITE AND READ IN CMT	DP
AUTO-POWER-OFF CHECK	MT
MEMORY LOOP CHECK	AP
KEY ENTRY CHECK	AP Y
DATA TRANSFER/RECEIVE THROUGH RS-232C PORT	KB
DATA RECEIVE	
DATA TRANSFER	ML
FDD READ/WRITE CHECK	MS
	FD

Note: This test program cannot check the internal main RAM of 8K bytes.

8-2. PREPARATION

Before start this program, you must have a FP-200 to be checked, a working FP-1021FD, AC adaptor AD4180, and the diskette of the test program ready before proceeding to the steps below.

2-1. First remove the power battery pack from the unit and insert the pack from FDD unit FP-1021FD.

2-2. Connect the power jack from the adaptor into the unit. The female jack locates on your right hand.

2-3. Turn on the power of the FP-1021FD first, then the FP-200.

2-4. Set the dialect selection switch to BASIC.

2-5. Insert the test program diskette slowly into the drive unit. This diskette must remain in operation in the drive unit until the testing ends.

OPERATION

INDICATION ON LCD

Enter the following commands and keys to begin the program.

RESET ↵
AREA 1000 ↵
MOUNT 1 ↵
LOAD "TP", R ↵

After about 20 seconds, the indication shown in Fig. 1 appears on the LCD.

Note: Entering a command code only causes its program run to be effective when the indication on the LCD is shown as in Fig. 1. When the indication shows other than this, enter LOAD "command code no." then press the ↵ key to load the program from the test program diskette.

PX-1 TEST PROGRAM
VER. 1.1
COMMAND = _

Fig. 1

MASK ROM CHECK

Enter MR ↵

This command checks the 32K mask ROM, (0000H – 7FFFH).
If result is correct, the indication shows "OK"; if not, the indication shows "ERROR" and its different sum amount.

* MASK ROM CHECK *
******* OK *******
END? Y OR N = _

Fig. 2

ROM PACK (FP-205ROM) CHECK

Enter ER ↵

This command checks carry-add sum amount in the 8-K byte ROM pack (FP-205ROM) (E000H – FFFH) in the compartment.

DATA WRITE IN RAM PACK

Enter CW ↵

This command writes the formatted data in a designated RAM pack (FP-201RAM) by you from 1 to 3 in the compartment. As soon as the indication shown on right Fig. 3 appears, enter the last installed RAM pack (number 1, 2, or 3). Numbers other than these three are not accepted and the computer holds the waiting condition.
Writing ends at once and no result is indicated in this mode.

Fig. 4 shows data is written in RAM pack no. 1 and the end message.

INDICATION ON LCD

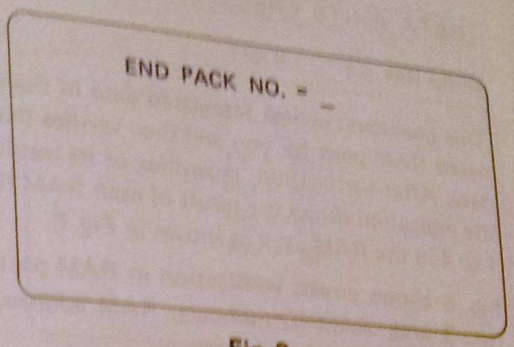


Fig. 3

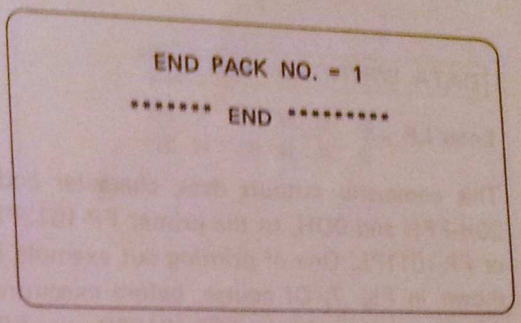


Fig. 4

DATA VERIFICATION IN RAM PACK

1. Enter CR ↵
2. Enter RAM pack number ↵

This command verifies data in a RAM pack (FP-201RAM) that is written by the command CW and indicates its result.
If verification is correct, then no result is displayed, but when the verification is not correct, the indication shows error address from the starting address of that RAM pack memory address to the last memory address, twice wrong read data and original data respectively from left to right on the LCD as shown in Fig. 5.

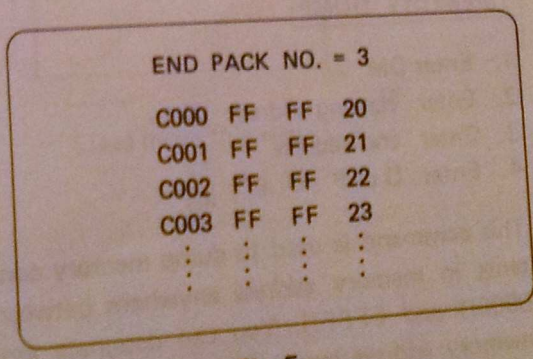


Fig. 5

DATA WRITE CHECK IN RAM PACK

Enter RM ↵

This command writes formatted data in designated RAM pack by you and then verifies that data. After verification, regardless of its result, the indication shows the result of each RAM IC 1 to 4 in the RAM pack as shown in Fig. 6.

Fig. 6 shows erratic verification in RAM pack No. 3 and, RAM IC numbers, RAM address, erratic data, and original data.

```
PACK NO. = 3

RAM 1: E000  FF  FF  00
RAM 2: E800  FF  FF  00
RAM 3: F000  FF  FF  00
RAM 4: F800  FF  FF  00

PACK NO. = _
```

Fig. 6

DATA WRITE IN PRINTER

Enter LP ↵

This command outputs data, character code 20H-FFH and 0DH, to the printer FP-1012PR or FP-1011PL. One of printing out example is shown in Fig. 7. Of course, before executing this command, printer FP-1012PR or FP-1011PL must be connected while all units are turned off.

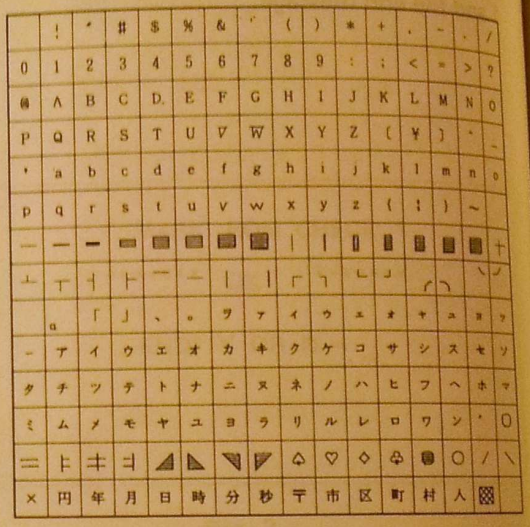


Fig. 7 PRINTING OUT ON FP-1011PL

MEMORY DUMP

1. Enter DM ↵
2. Enter starting address ↵
3. Enter end address ↵
4. Enter D or P ↵

This command is used to dump memory contents in memory address anywhere between 0000H and FFFFH. You can designate any memory address area and also select the output device, a display or printer. Data is printed by two digits hexadecimal notation.

First enter start address then end memory address, and D or P, referring as to the display or the printer, consecutively.

```
START ADDRESS = FFF0

END ADDRESS = FFFF

[D] OR [P] ?D

FFF0  FF  FF  FF  FF

FFF4  FF  FF  FF  FF
```

Fig. 8

SETTING AND COUNTING TIME

Enter TM ↵
Enter year (two digits) ↵
Enter month (two digits) ↵
Enter date (two digits) ↵
Enter hour (two digits) ↵
Enter minute (two digits) ↵
Enter second (two digits) ↵

After entering data for the year, month, date, hour, minute, and second, in proper number, be sure that indication shows all these data and counting of time on the LCD as shown in Fig. 10.

To terminate this counting mode, enter ↵ and Y.

DISPLAY CHECK

Enter DP ↵

This command draws two vertical lines, one from left to the center and the other from the center to right, simultaneously first, then two horizontal lines, one from top to the center and the other from the center to bottom, simultaneously, so that each dot on the LCD can be checked, it takes about 40 seconds to complete the operation.

INDICATION ON LCD

Fig. 9

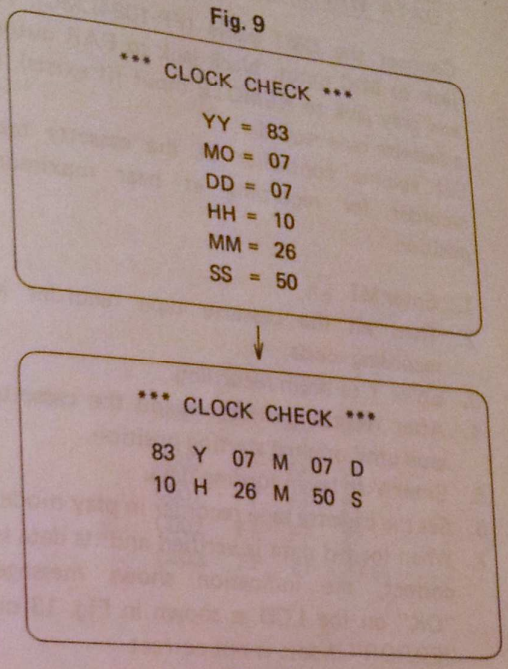


Fig. 10

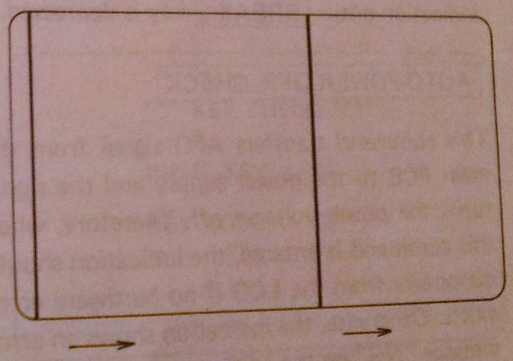


Fig. 11

DATA WRITE AND READ IN CMT

Connect the CMT cable (FP-1084CMC), red jack to MIC input, black jack to EAR output and gray jack to REMOTE input (if exists), to a cassette tape recorder.
Set volume controller of the cassette tape recorder for recording at near maximum position.

1. Enter MT ↵
2. Then set the cassette tape recorder in recording mode.
3. Enter Y to begin recording.
4. After recording ends, rewind the cassette tape until original starting position.
5. Enter Y to begin loading data.
6. Set the cassette tape recorder in play mode.
7. When loaded data is verified and its data is correct, the indication shows message "OK" on the LCD as shown in Fig. 13 or "ERROR" if data is not correct.

When the cable is not properly plugged in, the indication does not show any message for its improper connection but it holds save or load indication until BREAK key is depressed.

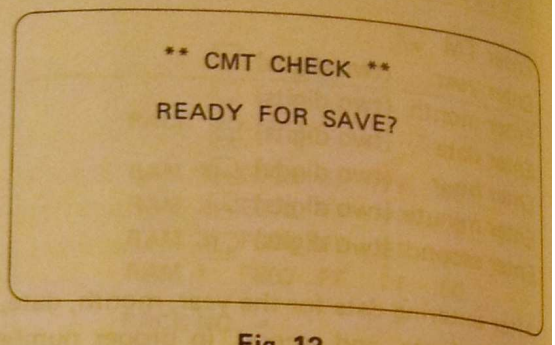


Fig. 12

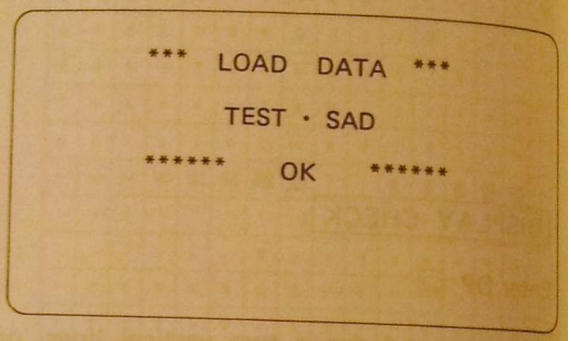


Fig. 13

AUTO-POWER-OFF CHECK

This command transfers APO signal from the main PCB to the power supply and the signal turns the power voltages off. Therefore, when this command is entered, the indication should disappears from the LCD if no hardware error exists. Otherwise, the indication shows an error message "NG" on the LCD as shown in Fig. 14.

1. Enter LOAD "AP" ↵
2. Turn the power of FP-200 and FP-1021FD off.
3. Unplug the power jack of the adaptor from the unit and the pack of FP-1021FD (disconnect FP-1021FD from FP-200).
4. Install the battery pack for the power source.
5. Turn the power of FP200 on and enter RUN ↵.
6. Enter AP ↵

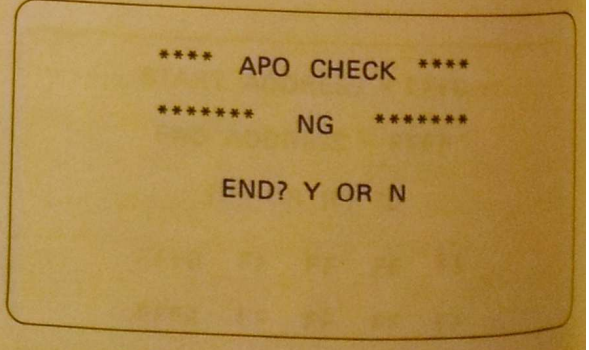


Fig. 14

To terminate this mode enter BREAK key, or Y to proceed to next check operation, memory loop.

Note: From step 5, the adaptor should not be used. Use the battery pack instead.

MEMORY LOOP CHECK

This command verifies data in a RAM pack loop which is written by the command CW, and shows its result in the same manner that the command CR does.

1. Enter AP ↵ Y ↵
2. Enter Y
3. Enter RAM pack number 1 or 2 or 3 ↵

This mode does not end by itself. To terminate this mode, depress BREAK key.
When this check operation is succeeded from the auto-power-off check, you do not need to enter AP ↵ , simply enter Y only.

Indication in Fig. 15 shows that data in RAM pack 3 is not verified and the operation is in loop mode.

```
END PACK NO. = 3

C000   FF   FF   20
C001   FF   FF   21
C002   FF   FF   22
C003   FF   FF   23
```

Fig. 15

KEY ENTRY CHECK

This command allows you to enter keys from the keyboard and the indication shows you the entered key symbol on top of it and its character code. It can confirm both key entries, lower case and upper case characters.

Enter KB ↵ and keys

To terminate this mode, enter ↵ key or BREAK key.

```
*** KEY CHECK ****

INPUT KEY  =  0

KEY CODE   =  30
```

Fig. 16

DATA TRANSFER/RECEIVE THROUGH RS-232C PORT

This check is used for data transfer and receive between two RS232C ports of FP-200. The data, 1, 2, 4, 8, 10, 20, 40, 80H, is transferred by the command MS and is received by the command ML.
Configuration for this check mode is that you must have another FP-200 with the "ML" program loaded and the receive side must be in receive mode to load data in (the command ML must be executed) before transferring data. In addition to above setting, you must make wiring between the two cables, FP-280RSC as shown in Fig. 17.

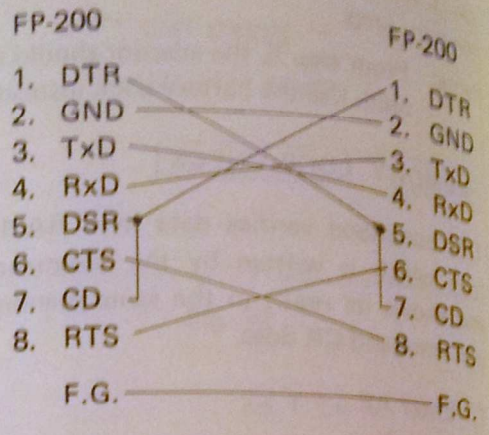


Fig. 17 WIRING FOR THE CHECK MODE

RECEIVE SIDE

1. Enter ML ↵ and Y (if both sides are ready)

After receiving data at the receive side, data is verified with original data and its result is indicated by message "OK" or "ERROR."

TRANSFER SIDE

2. Enter MS ↵ and Y (if both sides are ready)

FDD READ/WRITE CHECK

This command firstly formats a diskette and then write and read data in all sectors and tracks, 0 – 34.
During the operation, sector and track numbers where data is written and is read are shown on the LCD. When the operation ends, the result is indicated by "OK" for correct, or "ERROR" for erratic read/write operation.

1. Enter FD ↵
2. After the program is loaded, remove the test program diskette from the drive and insert a work diskette instead.
3. Enter Y when it is ready for formatting. The formatting should end in 20 seconds.
4. Then data is automatically written.

```
**** FDD CHECK ****

TRACK  = 34
SECTOR =  8

******   OK   ******

END? Y OR N = _
```

Fig. 18

9. SERVICE TOOLS AND TEST EQUIPMENT

Tools and equipment listed below are required to maintain and repair this computer unit accurately and promptly. Although most of the tools and equipment are probably available throughout the world, any tools or equipment not available from commercial sources in your local area can be obtained by contacting the overseas parts supply division, giving part code number, name, etc. Please allow four to five weeks for delivery from the date of your order.

Place order with: Casio Computer Co., Ltd.
20th Floor, Shinjuku-Sumitomo Bldg.
2-6, Nishi-Shinjuku, Shinjuku-ku
Tokyo 160, Japan
Telex: J26931 CASIO

SERVICE TOOLS

NAME	CODE NO.
1. PHILLIPS SCREWDRIVER, TYPE M2	00030563
2. PHILLIPS SCREWDRIVER, TYPE M3	00030564
3. FLAT SCREWDRIVER	00019650
4. CUTTERS	00019419
5. PLIERS	00019534
6. A PAIR OF TWEEZERS	00019418
7. SOLDERING IRON	00019652
8. SOLDER	00019401
9. SOLDER SUCKER	00019488
10. SODER WICK	00019400
11. LSI-REMOVING SOLDERING IRON UNTEX 25 (AC 100–117 V)	00019407
12. LSI-REMOVING SOLDERING IRON UNTEX 25 (AC 220-240 V)	00019594
13. LSI-REMOVING SOLDERING TIP (KM-813*1)	00019591
14. LSI-REMOVING SOLDERING TIP (KM-813*3)	00019585
15. TEST PROGRAM	
TEST EQUIPMENT	
1. OSCILLOSCOPE, 50-100 MHz WITH 3 PROBES	
2. MULTIMETER	00019458

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price J.F. Yen (¥) (FOB: JAPAN)	RANK
		MAIN P.C.B. (P1-1) ASSEMBLY C127-1					
☆	20001119	LSI (Timer)	RP5C01	1			B
☆	20007435	LSI (C-MOS ram)	TC5518BF-20	4			B
☆	20014491	LSI (Rom)	HN613256PC01	1			B
☆	20020334	LSI (Gate array)	μPD65010G-030	1			B
☆	20040076	LSI (CPU)	MSM80C85AGS	1			B
	21003247	MOS IC	TC4050BP	3			B
	21003867	C-MOS IC	TC40H002P	2			B
	21003875	MOS IC	TC40H000P	2			B
	21003905	C-MOS IC	TC40H032P	2			B
	21003948	MOS IC	TC40H368P	2			B
	21003990	MOS IC	TC40H139P	1			B
	21004002	MOS IC	TC50H000P	4			B
☆	21004111	MOS IC	TC40H245F	1			B
☆	21004120	MOS IC	TC40H008P	1			B
☆	21004138	MOS IC	TC50H001F	3			B
	21110949	Bipolar IC	HD74LS367P	5			B
	21112267	Bipolar IC	SN75189N	1			B
	21112275	Bipolar IC	SN75188N	1			B
	21208086	Linear IC	LM393P	1			B
☆	21800306	MOS IC	TC40H138P	1			B
	22003577	Transistor	2SA1015	2	10		B
	22202375	Transistor	2SC945	3	10		B
	23001021	Diode	1S2075K	11	10		B
	23209578	LED	LN28, CS	1	10		B
☆	25202155	Crystal oscillator	PX-1-6144	1	10		B
	26004918	Carbon film resistor	R-25-1K-J (1 Kohm, ¼ W)	1	10		X
	26005710	Carbon film resistor	R-25-2.2K-J (2.2 Kohm, ¼ W)	1	10		X
	26009715	Carbon film resistor	R-25-100K-J (100 Kohm, ¼ W)	2	10		X
	26010519	Carbon film resistor	R-25-220K-J (220 Kohm, ¼ W)	4	10		X
	26012112	Carbon film resistor	R-25-1M-J (1 Mohm, ¼ W)	5	10		X
	26007313	Carbon film resistor	R-25-10K-J (10 Kohm, ¼ W)	3	10		X
	26005515	Carbon film resistor	R-25-1.8K-J (1.8 Kohm, ¼ W)	4	10		X
	26010918	Carbon film resistor	R-25-330K-J (330 Kohm, ¼ W)	3	10		X
	26008719	Carbon film resistor	R-25-39K-J (39 Kohm, ¼ W)	1	10		X
	26006716	Carbon film resistor	R-25-5.6K-J (5.6 Kohm, ¼ W)	1	10		X

Notes: ☆: parts newly employed
Q'ty: quantity used per unit
*: minimum order per supply

Rank: A: Essential
B: Stock recommended
C: Less recommended
X: No stock recommended

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price J.F. Yen (¥) (FOB: JAPAN)	RANK
7☆	64000888	Key contact rubber B P1	C350-1	1			
8☆	64001078	Function button A P1	C465-1	4	10		X
9☆	64001086	Function button B P1	C466-1	8	10		X
10☆	64001094	Button spring P1	C471-1	2	10		X
11☆	64001141	Slide plate P1	C476-1	2	10		X
12☆	64001159	Slide cap P1	C477-1				X
13☆	64001299	Function button C P1	C484-1	1	10		
14☆	64300300	Keyboard sealed plate P1	C274A-1	1			X
15☆	64370081	Upper case sub assembly P1	C249B-1	1			X
16☆	64000861	Display window P1	C347-1	1			X
17☆	64001272	Decoration plate B P1	C482-1	1			X
		2. KEYBAORD P.C.B. (P1-E4) C243-1					X
	23003031	Diode	1S1588	16	10		B
☆	36120223	Terminal	2-4	1			X
☆	43080013	P.C.B. P1-E3	C388-1	1			X
☆	43080027	P.C.B. P1-E4	C129B-1	1			X
☆	64001205	PC joiner 2 P1	C480-2	1			X
☆	64001256	Joiner holder 5 P1	C481-5	2	10		X
☆	64001264	Joiner holder 6 P1	C481-6	1	10		X
☆	64003291	FFC joiner 2 P1	C479-2	1			X
		3. SLIDE BOARD SUB ASSEMBLY M41108-1					
☆	55801274	Ball bearing	SUS304	1	10		X
☆	69014972	Slide contact B	M4797B-1	1	10		X
	69100480	Slide spring	M4491-1	1	10		X
	69104010	Slide board	M4876-1	1	10		X
		4. RETURN BUTTON ASSEMBLY C364A-1					
☆	64000896	Return button P1	C351-1	1	10		X
☆	64001108	Plunger P1	C472-1	2	10		X
☆	64001116	Return button hung P1	C473-1	1	10		X
		5. SPACE BUTTON ASSEMBLY C363A-1					
☆	64000900	Space button P1	C353-1	1	10		X
☆	64001108	Plunger P1	C472-1	2	10		X

Notes: ☆: parts newly employed
Q'ty: quantity used per unit
*: minimum order per supply

Rank: A: Essential
B: Stock recommended
C: Less recommended
X: No stock recommended

Item	Code No.	Parts Name	Specification	Q'ty	*		Rank
☆	64001281	Space button ring P1	C483-1	1	10		X
☆	64001124	Space button hung P1	C474-1	1	10		X
☆	64001370	ASII key top set PIU	C251-1	1			X
☆	64001418	Control button set PIU	C382-2	1			X
		LOWER CASE ASSEMBLY C123-Z					
1	50411401	Screw, pan (+)	3 x 5	3	50		X
2	51111362	Tapping bind screw	3 x 8	5	50		X
3☆	51500938	Tapping bind screw	3 x 6, ZMC-3	1	50		X
4☆	51500946	Tapping bind screw	2.6 x 8, ZMC-3	2	50		X
5☆	51501101	Tapping bind screw	2.3 x 8, ZMC-3	2	50		X
6	51613031	Screw (+)	3 x 10, ZMC-3	2	50		X
7	51614071	Screw (+)	3 x 6	1	50		X
8☆	64000811	Battery cover P1	C341-1	1	10		C
9☆	64001396	Pack cover sub assembly P1	C361-1	1			X
10☆	64001981	Earth terminal P1	C4146-1	1			X
11☆	64001990	Terminal head P1	C4147-1	1	10		X
12☆	64003313	P label P1	C4179-1	1	10		X
13☆	64003321	Insulation plate P1	C4180-1	1	10		X
14☆	64003330	Press plate P1	C4181-1	1	10		X
15☆	64003364	S1 insulation plate P1	C4183-1	1	10		X
		OPERATING BATTERY BOX ASSEMBLY C362-1					
☆	64000802	Battery box P1	C241-1	1			X
☆	64000951	Battery spring 1 P1	C455-1	1	10		X
☆	64000969	Battery spring 2 P1	C456-1	1	10		X
☆	64000977	Battery spring 3 P1	C457-1	1	10		X
		LOWER CASE UNIT C244-Z					
1☆	30304055	Ferrite core	L5718 x 6 x 10	1	10		X
2☆	34205019	Power switch	S-1	1	10		X
3	35123148	Power jack	J-018	1	10		C
4☆	35900802	1L-G-2S connector	E31552-10	1			X
5☆	35900985	1L-G-5S connector	E31552-13	1			X
6☆	36603046	Terminal	2-4	2	10		X

Notes: ☆: parts newly employed
Q'ty: quantity used per unit
*: minimum order per supply

Rank: A: Essential
B: Stock recommended
C: Less recommended
X: No stock recommended

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price J.F. Yen (¥) (FOB: JAPAN)	RANK
☆	64001281	Space button ring P1	C483-1	1	10		X
☆	64001124	Space button hung P1	C474-1	1	10		X
☆	64001370	ASII key top set PIU	C251-1	1			X
☆	64001418	Control button set PIU	C382-2	1			X
LOWER CASE ASSEMBLY C123-Z							
1	50411401	Screw, pan (+)	3 x 5	3	50		X
2	51111362	Tapping bind screw	3 x 8	5	50		X
3☆	51500938	Tapping bind screw	3 x 6, ZMC-3	1	50		X
4☆	51500946	Tapping bind screw	2.6 x 8, ZMC-3	2	50		X
5☆	51501101	Tapping bind screw	2.3 x 8, ZMC-3	2	50		X
6	51613031	Screw (+)	3 x 10, ZMC-3	2	50		X
7	51614071	Screw (+)	3 x 6	1	50		X
8☆	64000811	Battery cover P1	C341-1	1	10		C
9☆	64001396	Pack cover sub assembly P1	C361-1	1			X
10☆	64001981	Earth terminal P1	C4146-1	1			X
11☆	64001990	Terminal head P1	C4147-1	1	10		X
12☆	64003313	P label P1	C4179-1	1	10		X
13☆	64003321	Insulation plate P1	C4180-1	1	10		X
14☆	64003330	Press plate P1	C4181-1	1	10		X
15☆	64003364	S1 insulation plate P1	C4183-1	1	10		X
OPERATING BATTERY BOX ASSEMBLY C362-1							
☆	64000802	Battery box P1	C241-1	1			X
☆	64000951	Battery spring 1 P1	C455-1	1	10		X
☆	64000969	Battery spring 2 P1	C456-1	1	10		X
☆	64000977	Battery spring 3 P1	C457-1	1	10		X
LOWER CASE UNIT C244-Z							
1☆	30304055	Ferrite core	L5718 x 6 x 10	1	10		X
2☆	34205019	Power switch	S-1	1	10		X
3	35123148	Power jack	J-018	1	10		C
4☆	35900802	1L-G-2S connector	E31552-10	1			X
5☆	35900985	1L-G-5S connector	E31552-13	1			X
6☆	36603046	Terminal	2-4	2	10		X

Notes: ☆: parts newly employed
Q'ty: quantity used per unit
*: minimum order per supply

Rank: A: Essential
B: Stock recommended
C: Less recommended
X: No stock recommended

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price J.F. Yen (¥) (FOB: JAPAN)	RANK
7 ☆	51500938	Bind tapping screw (+)	3 x 6, ZMC-3	2	50		X
8	51613040	Screw pan (+)	3 x 6, ZMC-3	2	50		X
9	55600201	Pony tie	P.T 75	6	10		X
10	60006091	Battery spring G67	A43656-1	1	10		X
11 ☆	60207666	Battery spring B2 G513	P409A-1	1	10		X
12 ☆	62693301	Battery spring 10A-A	A4353A-1	1	10		X
13 ☆	64000934	Power switch fixing metal P1	C453-1	1			X
☆	64300385	Power switch cap P1	C345A-1	1	10		X
14 ☆	64370120	Lower shield sub assembly PIU	C245B-2	1			X
☆	64001388	Upper shield sub assembly P1	C360-1	1			X

Notes: ☆ : parts newly employed
Q'ty : quantity used per unit
* : minimum order per supply

Rank: A : Essential
B : Stock recommended
C : Less recommended
X : No stock recommended

FP-205ROM (PX-107AA)

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price J.F. Yen (¥) (FOB: JAPAN)	RANK
	21003958	C-MOS rom IC	TC40H000F	1			B
	26004918	Carbon film resistor	R-25-1K-J (1 Kohm, ¼ W)	1	(10)		X
☆	27206069	Module resistor	EXB-P808-224M (220 Kohm, 50 W)	3	(10)		X
☆	28109024	Multilayer ceramic chip capacitor	ECU-XIH-104ZFM (0.1 μF, 50 V)	2	(10)		X
☆	28901437	Chip tantalum capacitor	ECSE1CB106	1	(10)		X
☆	43080020	P.C.B. P106/P107-1	C260-1	1			X
☆	64001574	Switch contact spring P105	C448-1	2	(10)		C
	63330000	Flat screw A-G3178	A45491-13	2	(50)		X
☆	64001523	Upper case P105/P107	C235-1	1			X
☆	64001531	ROM lower case P106	C236-1	1			X
☆	64001558	Interconnector P105	C446-1	1			C
☆	64001566	Pack fixing plate P105	C447-1	1			X
☆	64001582	Earth spring sub assembly	C451-1	1			X
☆	64001591	Earth spring fixing metal P105	C452-1	2	(10)		X
☆	64001621	Name label 3 P107	C4112-3	1	(10)		X

Notes: ☆ : parts newly employed
Q'ty : quantity used per unit
* : minimum order per supply

Rank: A : Essential
B : Stock recommended
C : Less recommended
X : No stock recommended

FP-201 RAM PACK (PX-105AA)

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price J.F. Yen (¥) (FOB: JAPAN)	RANK
☆	20007435	C-MOS RAM	TC5518BF-20	4			B
☆	(20020253)	C-MOS RAM	(μPD449G-1)	(4)			B
☆	21004146	MOS IC	TC40H139F	1			B
☆	28109024	Multilayer ceramic chip capacitor	ECU-XIH-104ZFM (0.1 μF, 50 V)	5	(10)		X
☆	28901437	Chip tantalum capacitor	ECSE1CB106	1	(10)		X
☆	43080019	P.C.B. P105-1	C259-1	1			X
☆	64001574	Switch contact spring P105	C448-1	2	(10)		C
	63330000	Flat screw A-G317B	A45491-13	2	(50)		X
☆	64001523	Upper case P105, 107	C235-1	1			X
☆	64001540	RAM lower case P105	C237-1	1			X
☆	64001558	Interconnector P105	C446-1	1			C
☆	64001566	Pack fixing plate P105	C447-1	1			X
☆	64001582	Earth spring sub assembly	C451-1	1			X
☆	64001591	Earth spring fixing metal P105	C452-1	2	(10)		X
☆	64001604	Name label 1 P105	C4112-1	1	(10)		X

FP-210KB (PX-511)

☆	00001251	PCB-CSO-16	56-8342	1			X
☆	00001252	DIN connector	56-8352	1			X
☆	00001253	Membrane CSO-16	56-8345	1			X
☆	00001254	Heat seal D-9	56-7378	1			X
☆	00001255	Holder metal	56-8142	1			X
☆	00001256	Holder metal fixing screw	56-0088	2	(50)		X
☆	00001257	KCD type keyboard switch (Small)	56-6442	14			X
☆	00001258	KCD type keyboard switch (Large)	56-6443	2			X
☆	00001259	Crank shaft CW	56-7841	2	(10)		X
☆	00001260	Crank guide CW	56-7842	4	(10)		X
☆	00001261	Key top set (Small) (15 pcs.)	56-3941	1 set			X

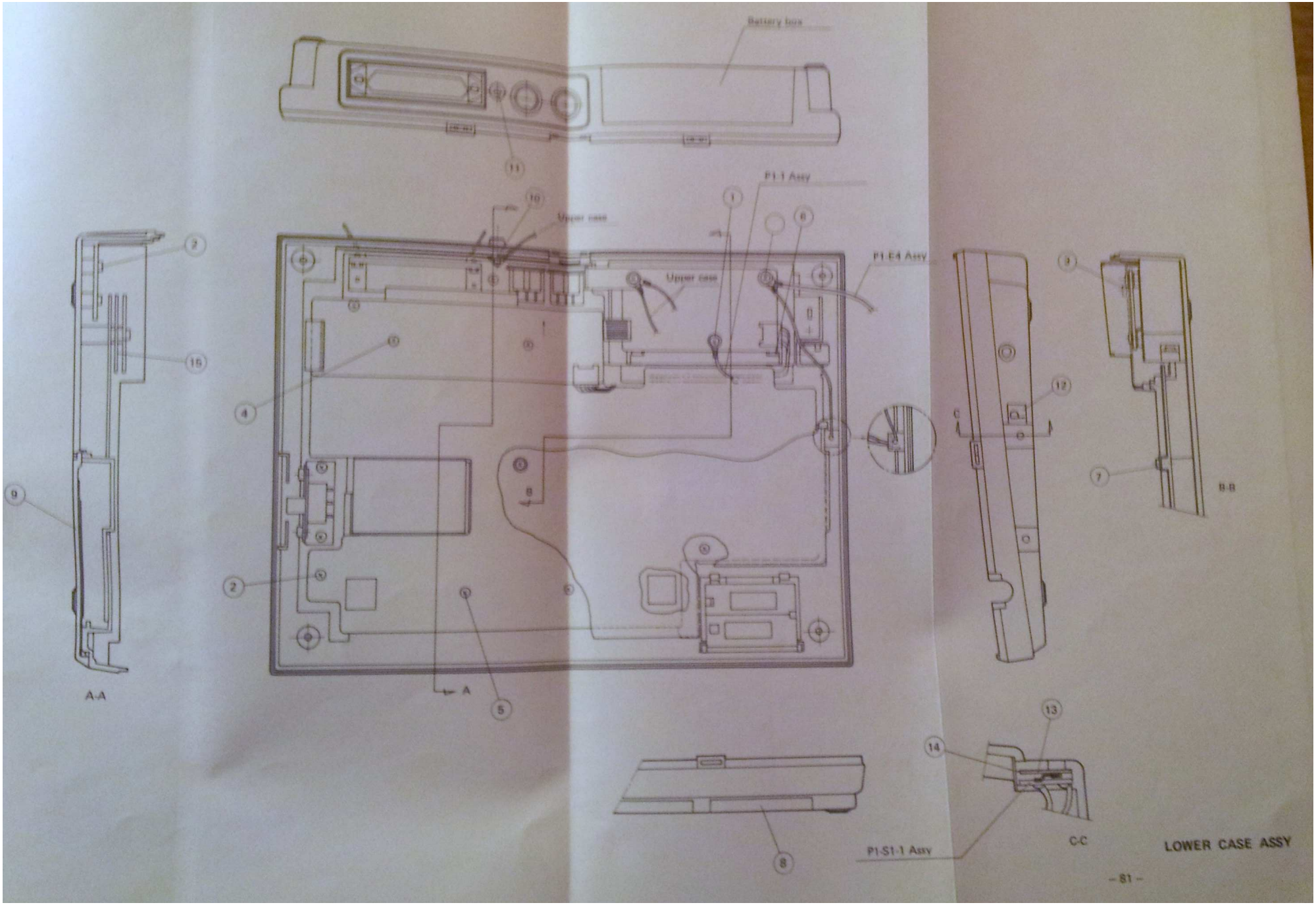
Notes: ☆: parts newly employed
Q'ty: quantity used per unit
*: minimum order per supply

Rank: A: Essential
B: Stock recommended
C: Less recommended
X: No stock recommended

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price J.F. Yen (¥) (FOB: JAPAN)	RANK
☆	00001262	Key top (Large)	D56-8876	1			X
☆	00001263	Upper case CSO-16	56-8257	1			X
☆	00001264	Lower case CSO-16	56-8258	1			X
☆	00001265	Cord holder CSO-16	56-8259	1			X
☆	00001266	Tapping screw M3 x 6	56-4965	2	(50)		X
☆	00001267	Tapping screw M3 x 8	56-0086	4	(50)		X
☆	00001268	Seal CSO-16	56-8349	1			X
☆	00001269	Rubber foot	56-8351	4	(10)		X

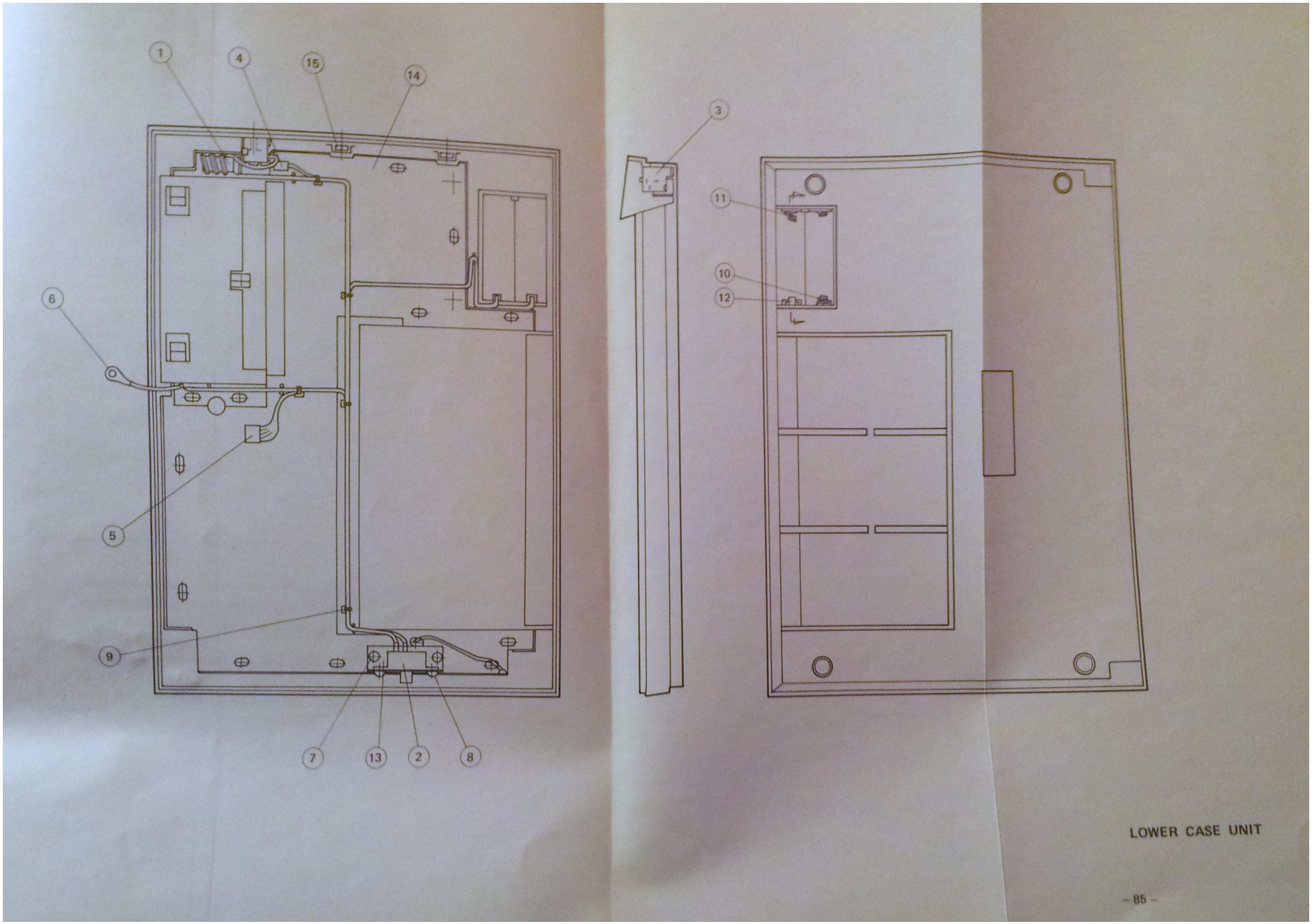
Notes: ☆ : parts newly employed
Q'ty : quantity used per unit
* : minimum order per supply

Rank: A : Essential
B : Stock recommended
C : Less recommended
X : No stock recommended



LOWER CASE ASSY

J Arrow view



LOWER CASE UNIT

Your constructive comments and suggestions concerning the contents of this service manual will assist us in our continuous efforts to improve the quality, the accuracy and the usefulness of this service manual.
If you have any comments and/or suggestions, please mail them to:

Casio Computer Co., Ltd.
Overases Service Division
20F, Shinjuku-Sumitomo Bldg.
2-6, Nishi-Shinjuku, Shinjuku-ku
Tokyo 160, Japan
Telex: J26931 CASIO

CASIO COMPUTER CO., LTD.

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